

35-45GHz Single Side Band Mixer Self biased

Preliminary

GaAs Monolithic Microwave IC

Description

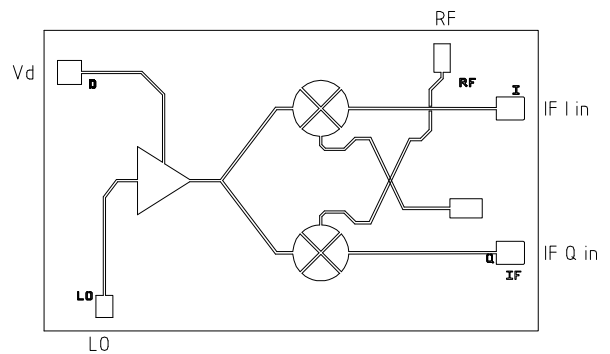
The CHM1294 is a multifunction chip (MFC) which integrates a self biased LO buffer amplifier and a sub-harmonically balanced diode mixer for 2LO suppression and image rejection. It is usable both for up-conversion and down-conversion.

It is designed for a wide range of applications, typically commercial communication systems for broadband local access. The backside of the chip is both RF and DC grounded. This helps to simplify the assembly process.

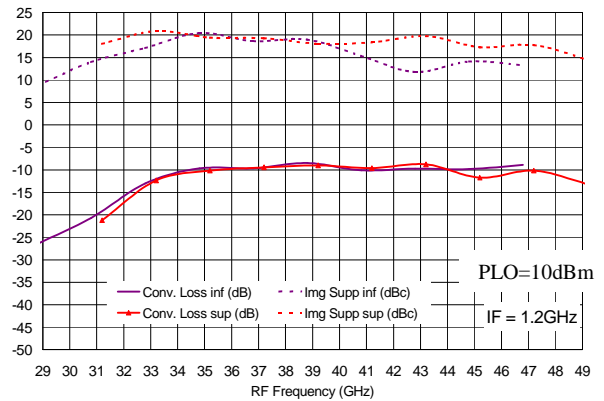
The circuit is manufactured with a pHEMT process, 0.25 μ m gate length. It is available in chip form.

Main Features

- Broadband performances: 35-45GHz
- 11dB conversion Loss
- 15dBc image rejection
- +10dBm LO input power
- +0dBm input power (1dB gain comp.)
- Power consumption 60mA@4V
- Chip size: 2.06 x 1.25 x 0.10mm



Up converter, Infradyne & supradyn mode



Main Characteristics

Tamb. = 25°C

	Parameter	Min	Typ	Max	Unit
F_{RF}	RF frequency range	35		45	GHz
F_{LO}	LO frequency range	16		24	GHz
F_{IF}	IF frequency range	DC		3	GHz
L_c	Conversion Loss		11		dB

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!

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Electrical Characteristics for Broadband Operation

Tamb = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
F _{LO}	LO frequency range	16		24	GHz
F _{IF}	IF frequency range	DC		3	GHz
L _c	Conversion Loss		11		dB
P _{LO}	LO Input power		+10		dBm
2xLO Leak	2xLO Leakage (for P _{LO} = +10dBm)		-35		dBm
Img Rej	Image Rejection (1)		15		dBc
P1dB	Input power at 1dB compression		+0		dBm
LO Match	LO VSWR*		2.0:1		
RF Match	RF VSWR*		2.0:1		
IF Match	IF VSWR*		2.0:1		
Vd	Drain bias supply		4		V
Id	Bias current		60		mA

(1) With external quadrature hybrid coupler (reference on request). The minimal value depends on the quality of the external quadrature combiner.

* A bonding wire of typically 0.1 to 0.15nH will improve the accesses matching.

Absolute Maximum Ratings

Tamb. = 25°C (1)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4.5	V
Id	Drain bias current	90	mA
P _{LO}	Maximum LO input power	15	dBm
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +125	°C

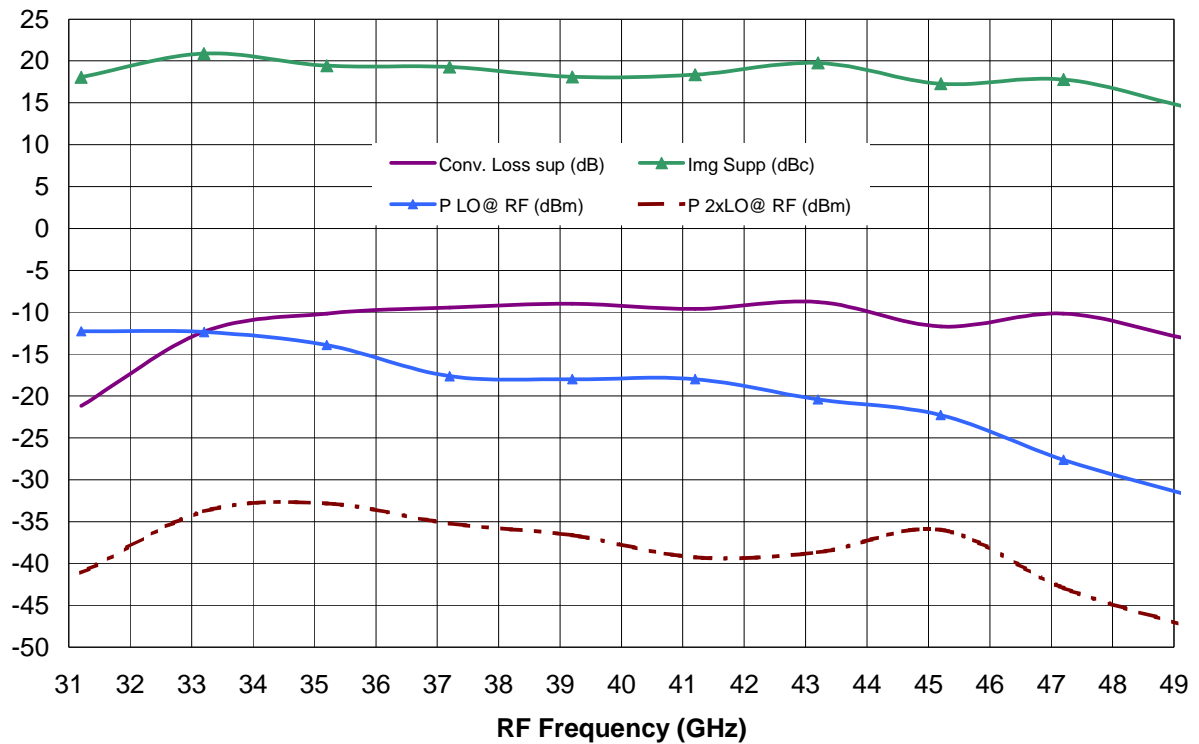
(1) Operation of this device above anyone of these parameters may cause permanent damage.

Typical on wafer measurement

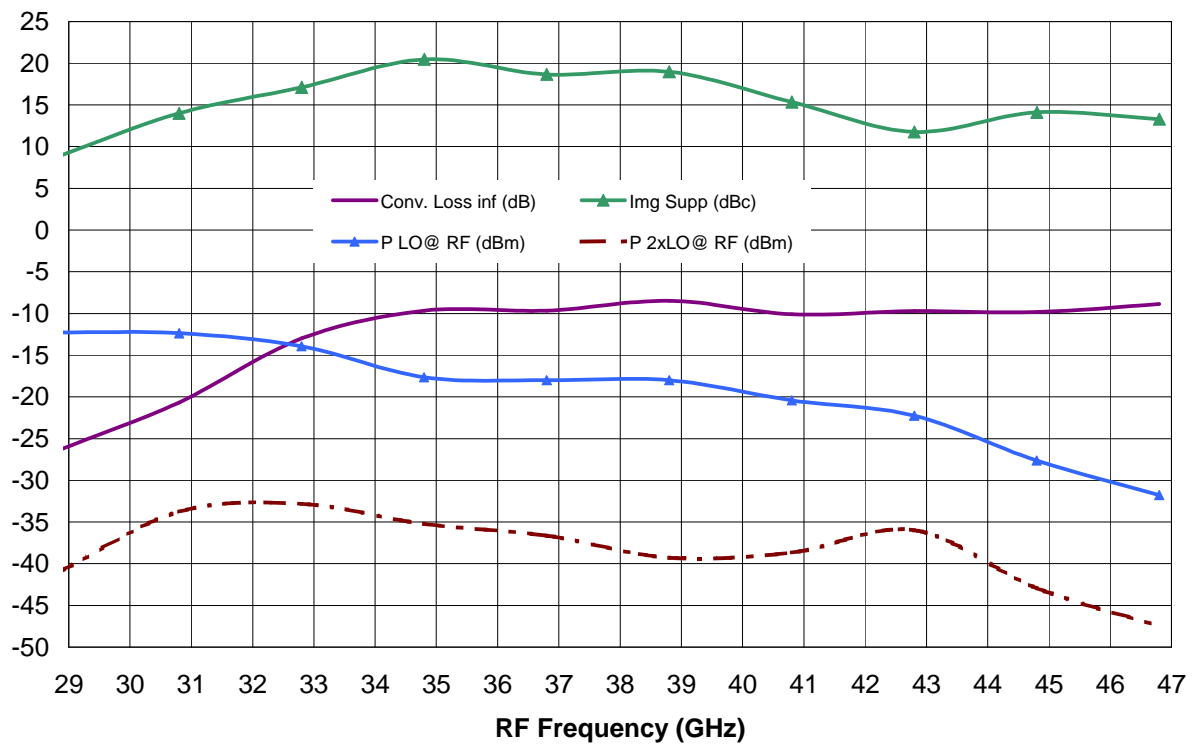
T_{amb} = 25°C, V_d = 4V, I_d = 60mA, Freq IF = 1.2GHz, P_{LO} = 10dBm

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Up Converter in Supradyne mode

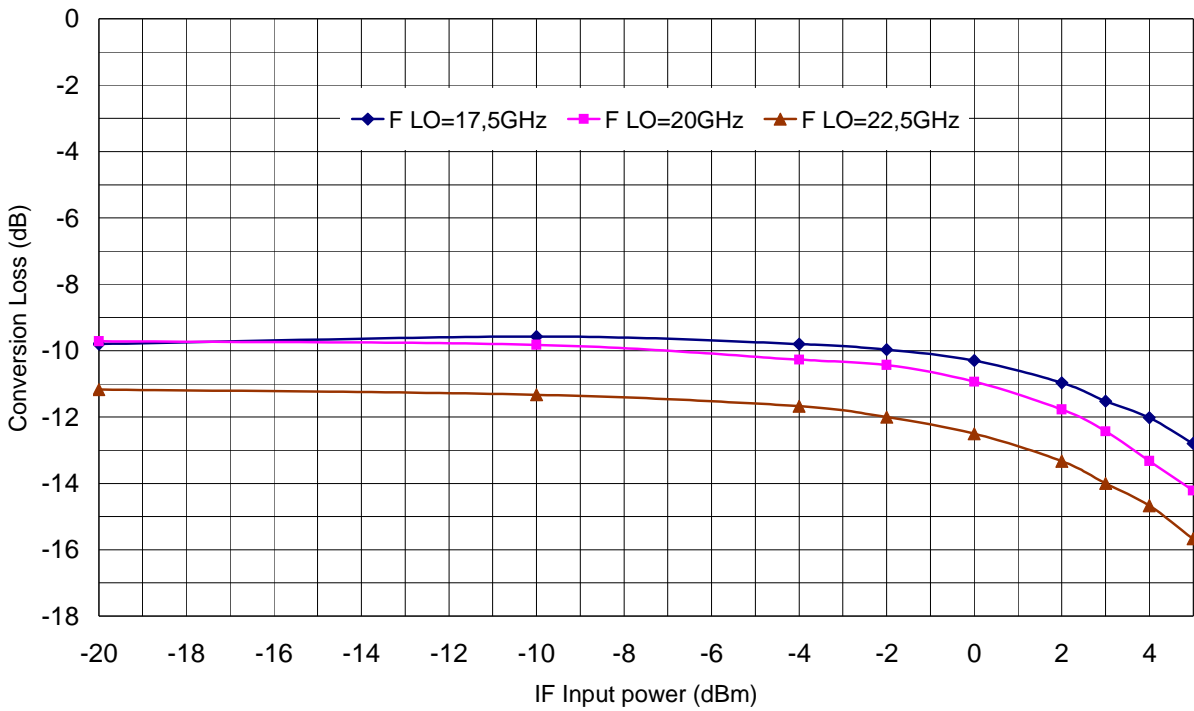


Up Converter in Infradyne mode

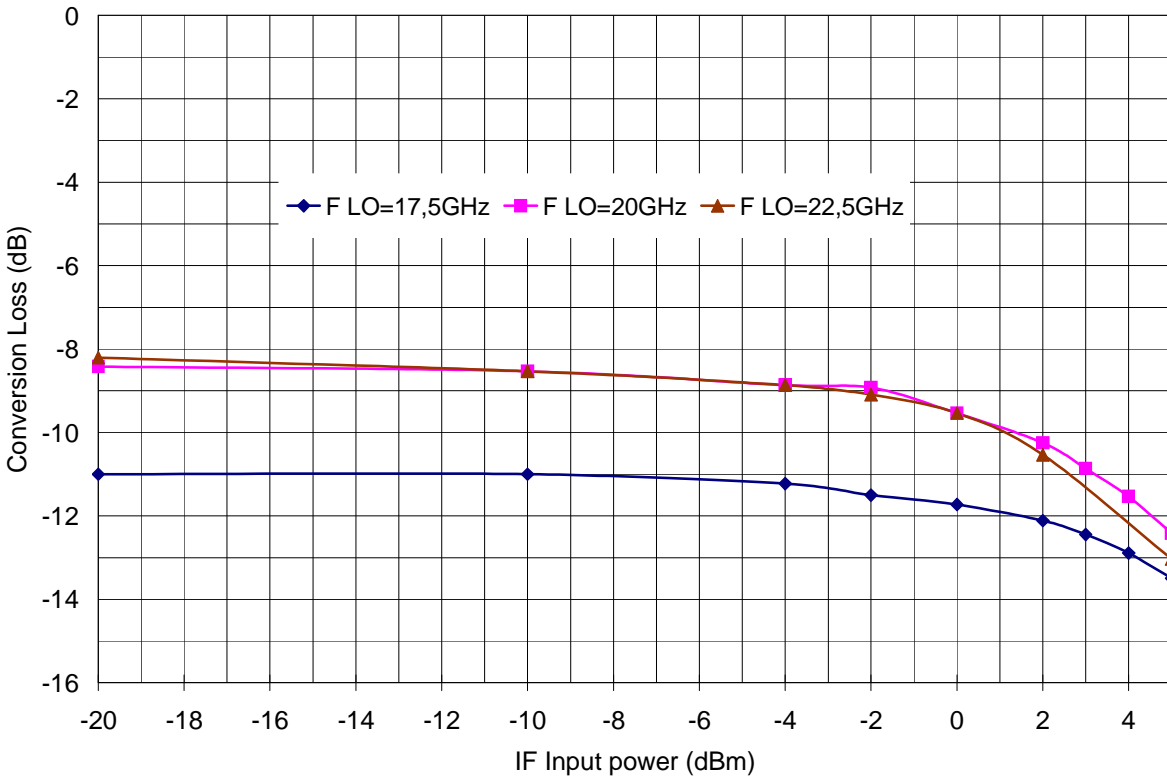


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Up Converter compression in Supradyne mode

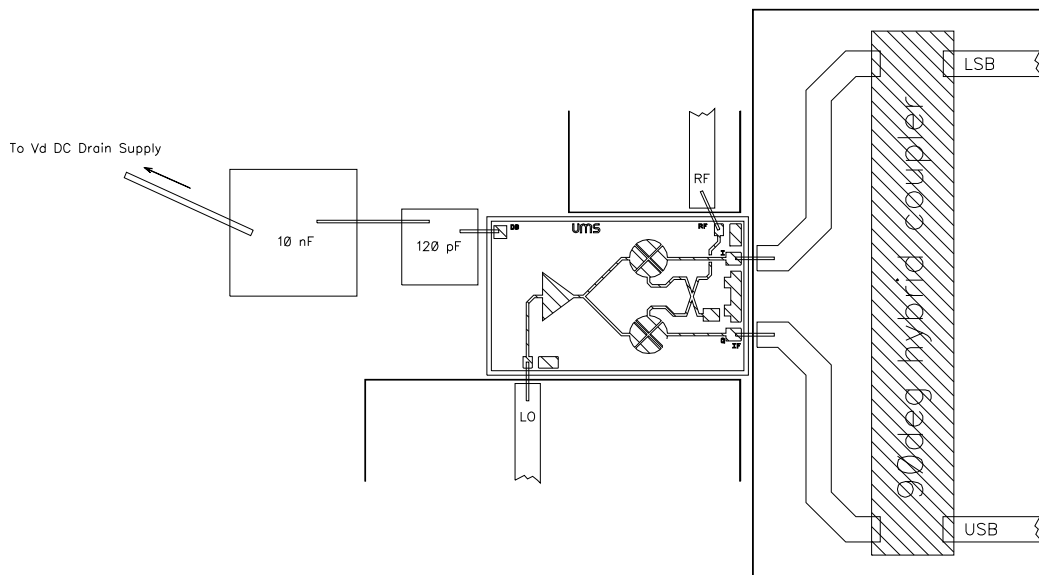


Up Converter compression in Infradyne mode

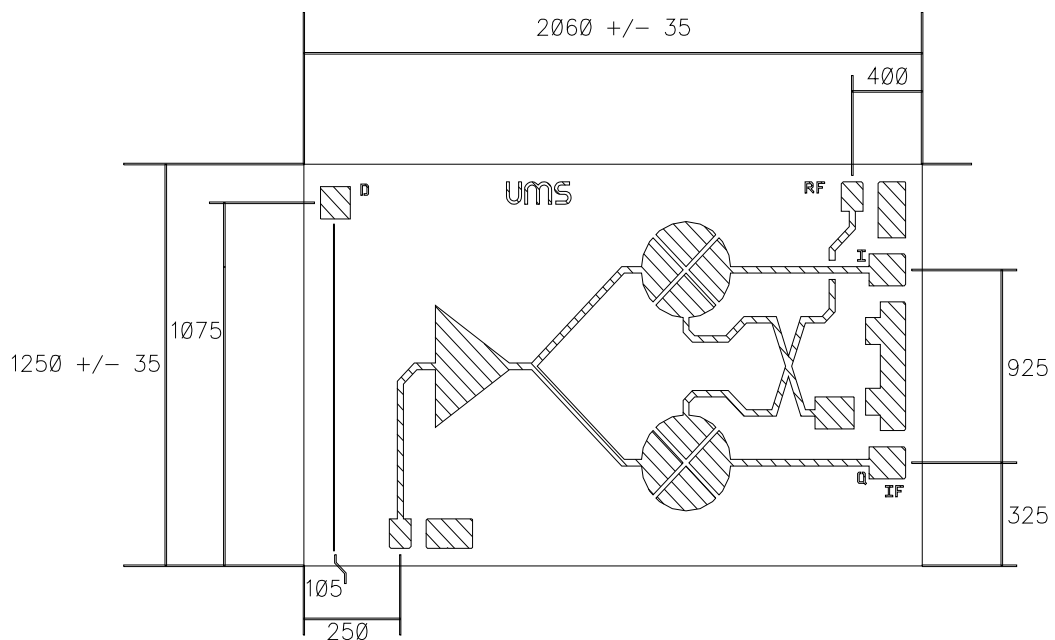


Chip Assembly and Mechanical Data

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Note: Supply feed should be capacitively bypassed. 25µm diameter gold wire is recommended



Chip Mechanical Data and Pin references

(Chip thickness: 100µm. All dimensions are in micrometers)

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Ordering Information

Chip form: CHM1294-99F/00

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