

55-65GHz Single Side Band Mixer

GaAs Monolithic Microwave IC

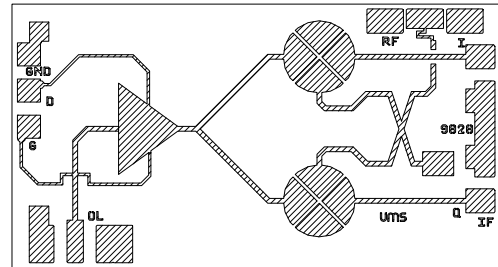
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Description

The CHM1298 is a multifunction chip (MFC) which integrates a LO buffer amplifier and a sub-harmonically balanced diode mixer for 2LO suppression and image rejection. It is usable both for up-conversion and down-conversion. It is designed for a wide range of applications, from military to commercial communication systems. The backside of the chip is both RF and DC grounded. This helps to simplify the assembly process.

The circuit is manufactured with a pHEMT process, 0.25 μ m gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is available in chip form.



Main Features

- Broadband performance: 55-65GHz
- 12dB conversion Loss
- 10dBc image rejection
- +10dBm LO input power
- +0dBm input power (1dB gain comp.)
- DC power consumption, 90mA @ 3.5V
- Chip size: 2.10 x 1.17 x 0.10mm

Main Characteristics

Tamb. = 25°C

Symbol	Parameter	Min	Typ	Max	Unit
F _{RF}	RF frequency range	55		65	GHz
F _{LO}	LO frequency range	27.5		32.5	GHz
F _{IF}	IF frequency range	DC		5	GHz
L _c	Conversion Loss		12		dB

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!

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Electrical Characteristics

Tamb = +25°C, Vd = 3.5V

Symbol	Parameter	Min	Typ	Max	Unit
F _{RF}	RF frequency range	55		65	GHz
F _{LO}	LO frequency range	27.5		32.5	GHz
F _{IF}	IF frequency range	DC		5	GHz
L _c	Conversion Loss		12		dB
P _{LO}	LO Input power		+10		dBm
2xLO Leak	2xLO Leakage (for P _{LO} = +5dBm)		-35		dBm
Img Rej	Image Rejection (1)		10		dBc
P1dB	Input power at 1dB gain compression		+0		dBm
P03	Input power at 3dB gain compression		+2		dBm
IP3	Input 3 rd order intercept point		+8		dBm
LO Match	LO Matching		2.0:1		
RF Match	RF Matching		2.0:1		
IF Match	IF Matching		2.0:1		
I _d	Bias current		90		mA

(1) With external quadrature hybrid coupler (reference on request)

A wire bond of typically 0.1 to 0.15nH will improve the input and output matching.

Absolute Maximum Ratings

Tamb = +25°C

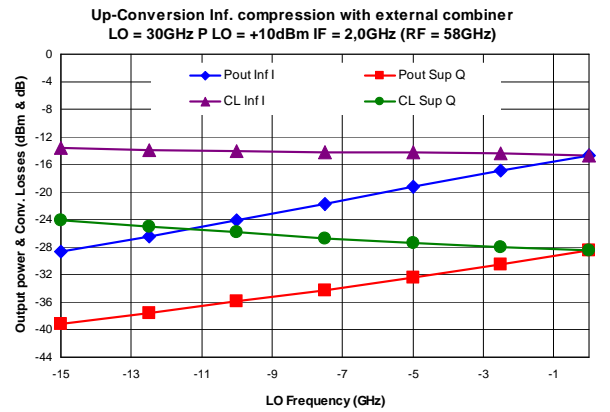
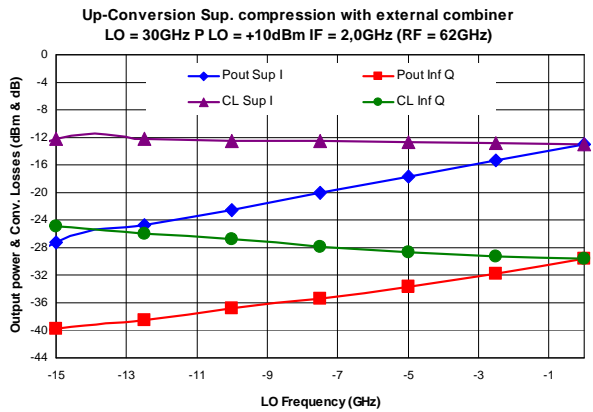
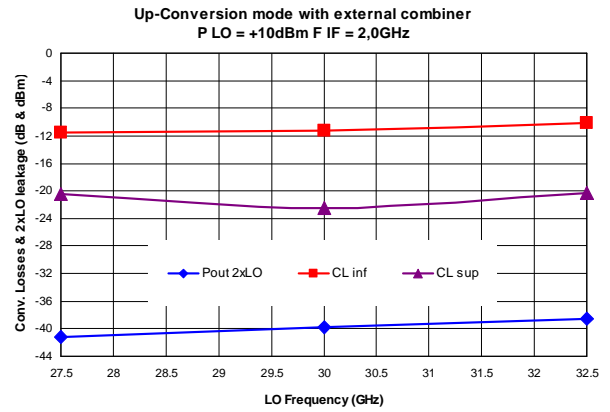
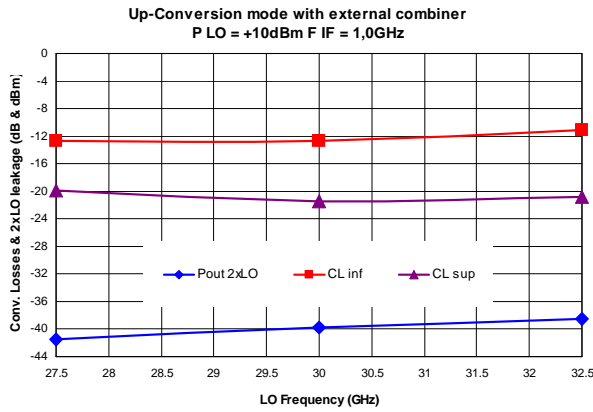
Symbol	Parameter	Values	Unit
V _d	Drain bias voltage	4.0	V
I _d	Drain bias current	150	mA
T _a	Operating temperature range	-40 to +85	°C
T _{stg}	Storage temperature range	-55 to +125	°C

(1) Operation of device above any of these parameters may cause permanent damage.

Typical On-wafer Measurements in Up-Conversion mode with external combiner

Bias conditions: $T_{amb} = +25^{\circ}C$, $V_d = 3.5V$, $I_d = 90mA$

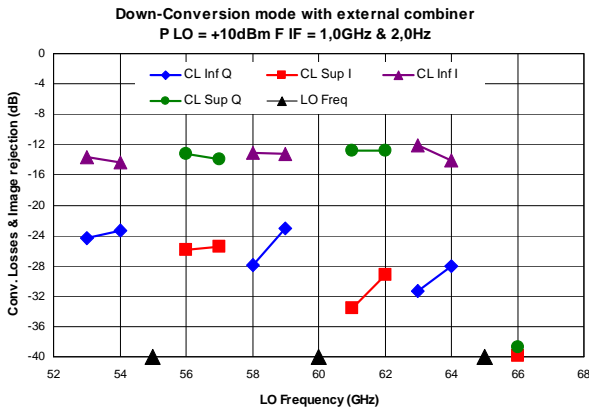
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Typical On-wafer Measurements in Down-Conversion mode with external combiner

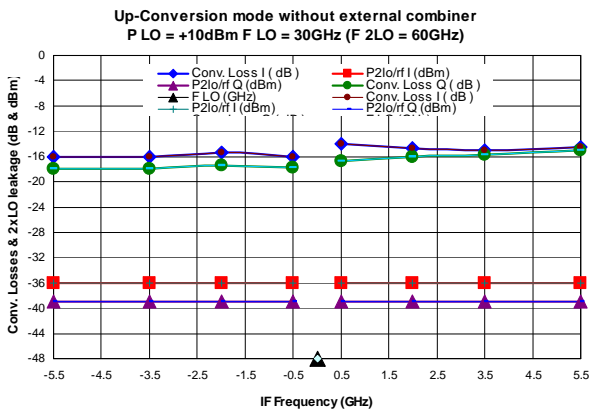
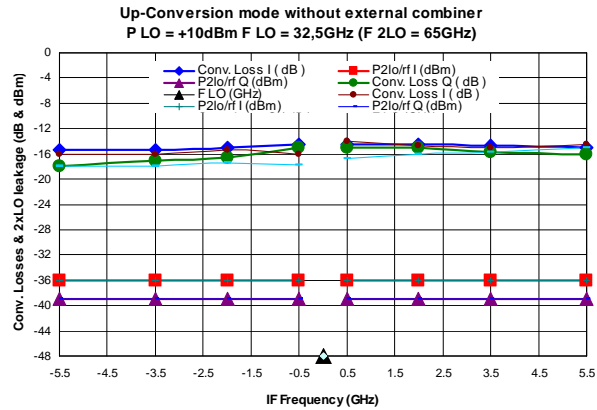
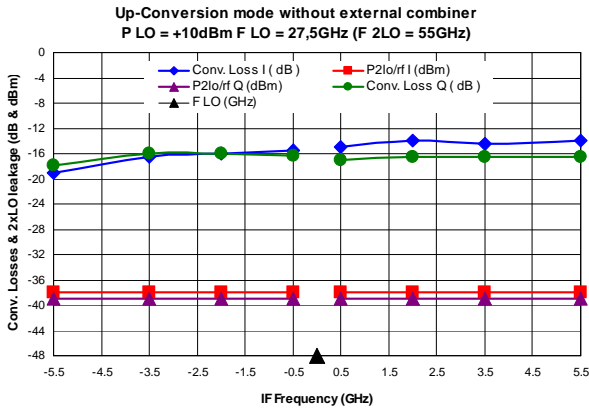
Bias conditions: $T_{amb} = +25^{\circ}\text{C}$, $V_d = 3.5\text{V}$, $I_d = 90\text{mA}$

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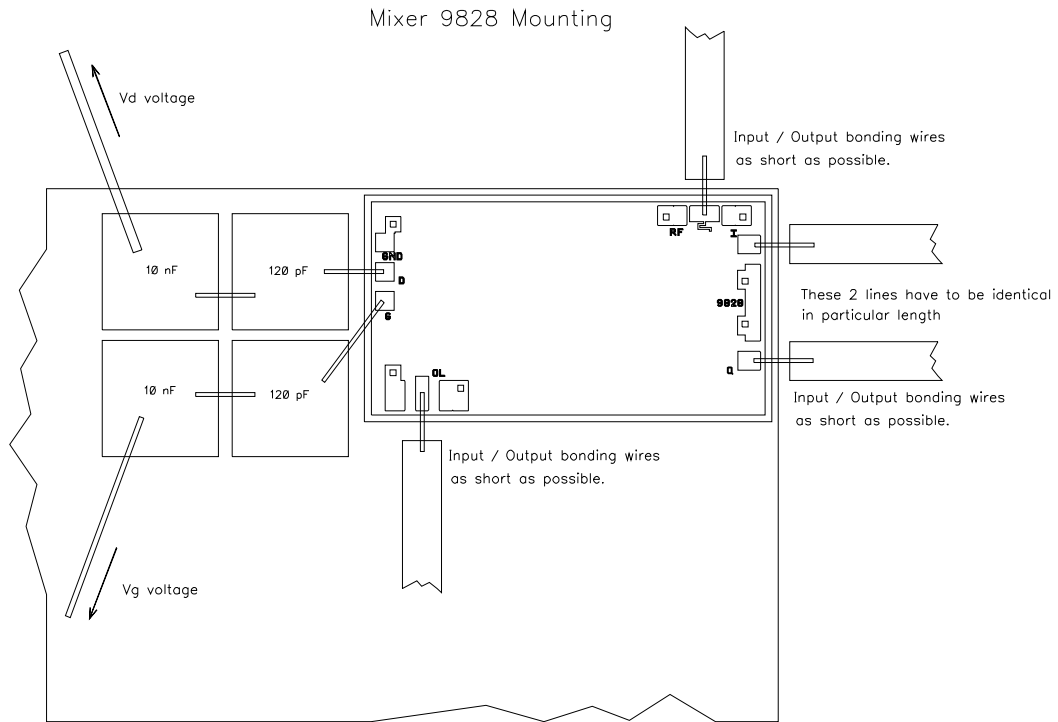
Typical On-wafer Measurements in Up-Conversion mode without external combiner

Bias conditions: $T_{amb} = +25^{\circ}\text{C}$, $V_d = 3.5\text{V}$, $I_d = 90\text{mA}$



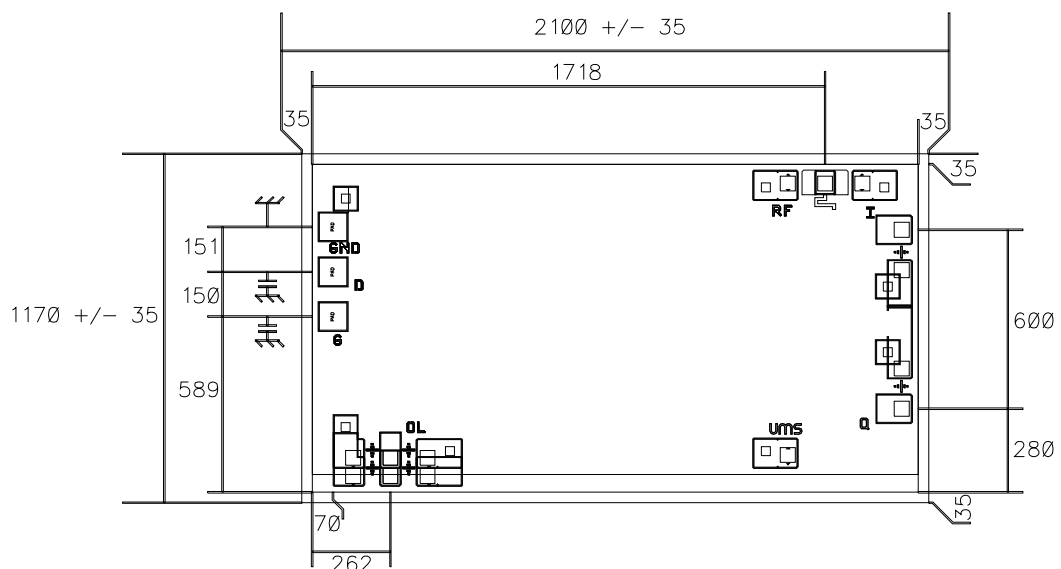
Chip Assembly and Mechanical Data

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Note: Supply feed should be capacitively bypassed. 25µm diameter gold wire is to be preferred.

It is necessary to use an external hybrid quadrature combiner on the IF ports if the image rejection functionality is required.



Bonding pad positions.
(Chip thickness: 100µm. All dimensions are in micrometers)

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Ordering Information

Chip form: CHM1298-99F/00

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