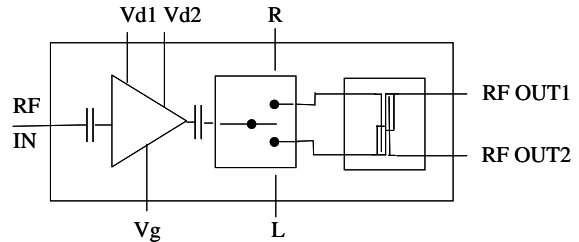


6-18GHz Dual Port Driver Amplifier

GaAs Monolithic Microwave IC

Description

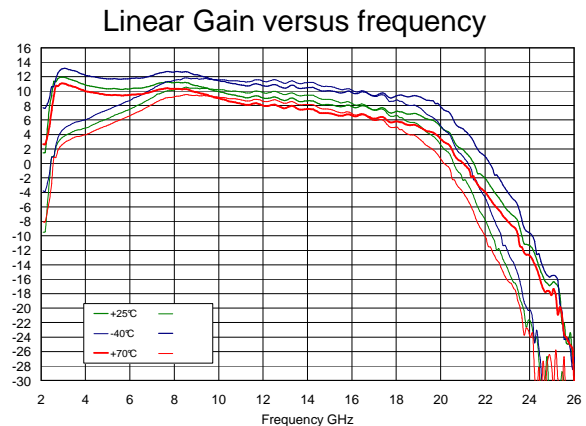
The CHA3517-99F is composed by a two stage travelling wave amplifier followed by a Single Pole Double Through (SPDT) switch and a lange coupler. It is designed for wide band applications such as test or defense. The backside of the chip is both RF and DC grounded. This helps to simplify the assembly process.



The circuit is manufactured with a pHEMT process, 0.25 μ m gate length, via holes through the substrate, air bridges and electron beam gate lithography. It is available in chip form.

Main Features

- 6-18GHz frequency range
- 18dBm saturated output power
- 8dB linear gain
- DC power consumption, 300mA @ 7V
- Chip size: 3.10x3.10x0.07mm



Main Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	6		18	GHz
Gain	Small signal gain		8		dB
Psat	Saturated Output power (both outputs)		18		dBm

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!

Main Characteristics

Tamb.= +25°C, Vd1= Vd2= 7V, Vg tuned for Id= 300mA

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range ⁽¹⁾	6		18	GHz
G	Small signal gain		8		dB
P1dB	Output power at 1dB gain compression (both outputs)		17		dBm
Psat	Saturated Output power (both outputs)		18		dBm
VSWRin	Input VSWR ⁽¹⁾		2.4:1		
VSWRout	Output VSWR ⁽¹⁾		2.0:1		
Vd	Drain bias DC voltage		7		V
Id	Bias current @ small signal		300		mA
Vc	Control voltage for SPDT (pads R & L)	-5		0	V

(1) These values are representative for on-wafer measurements that are made without bonding wires at the RF ports.

A bonding wire of typically 0.1 to 0.15nH will improve the matching at the accesses.

Absolute Maximum Ratings

Tamb.= +25°C ⁽¹⁾

Symb ol	Parameter	Values	Unit
Vd	Drain bias voltage	+8V	V
Id	Drain bias current	350	mA
Vg	Gate bias voltage	-2 to +0.4	V
Vc	Attenuator bits control voltage	-7 to +0.6	
Pin	Maximum peak input power overdrive ⁽²⁾	+20	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +70	°C
Tstg	Storage temperature range	-55 to +155	°C

⁽¹⁾ Operation of this device above any one of these parameters may cause permanent damage.

⁽²⁾ Duration < 1s.

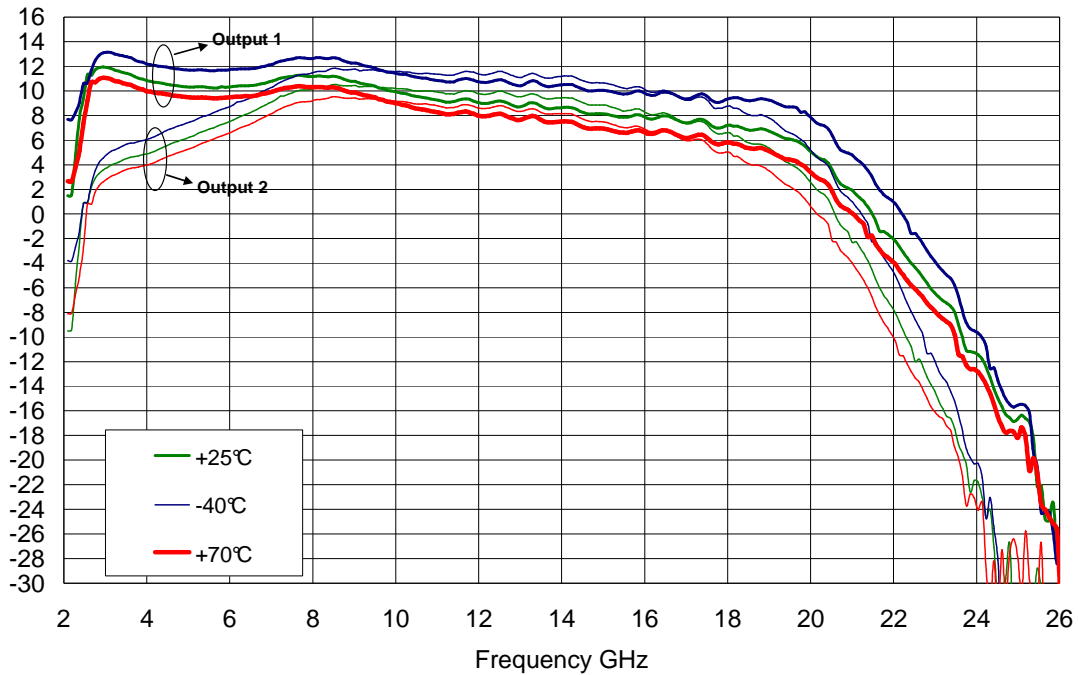
SPDT switch Control interface

	SPDT voltage Control (V)	
	R	L
RF OUT 1	-5	0
RF OUT 2	0	-5

Typical Test Fixture Measurements

Tamb.= +25°C, Vd = 7V, Vg tuned for Id = 300mA

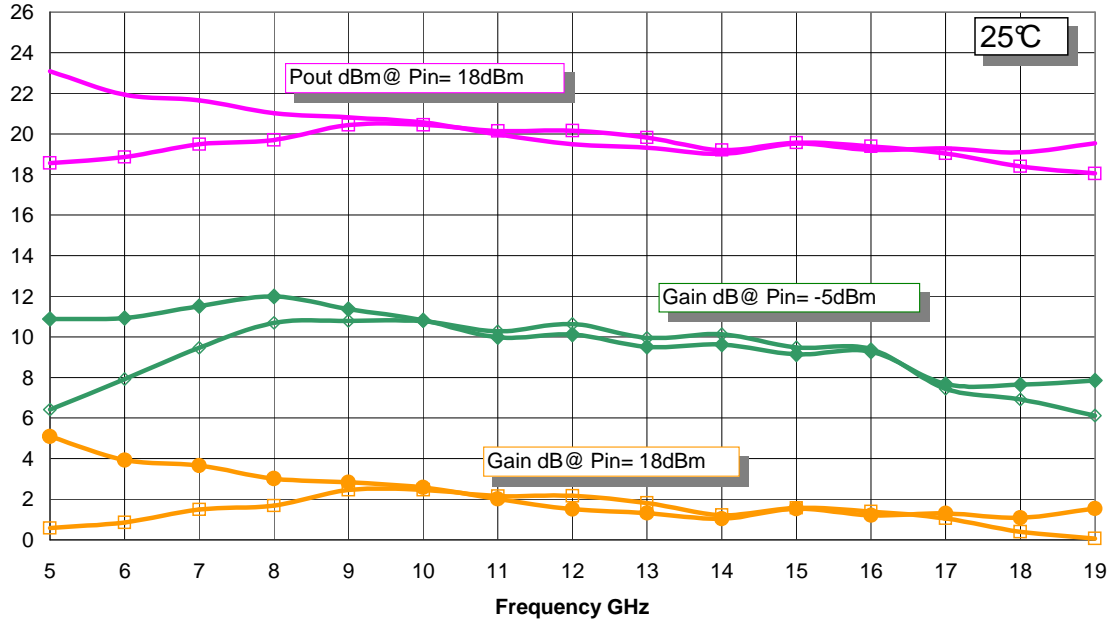
Linear Gain versus frequency in the two SPDT switch configurations



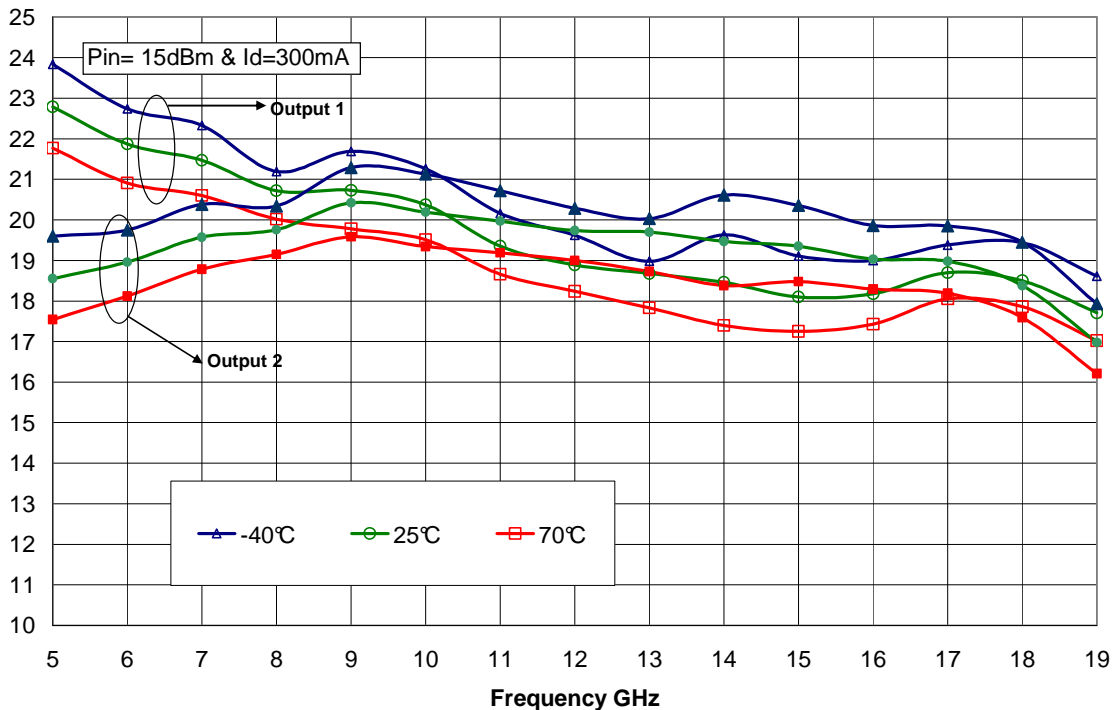
Typical Test Fixture Measurements

Tamb.= +25°C, Vd = 7V, Vg tuned for Id = 300mA

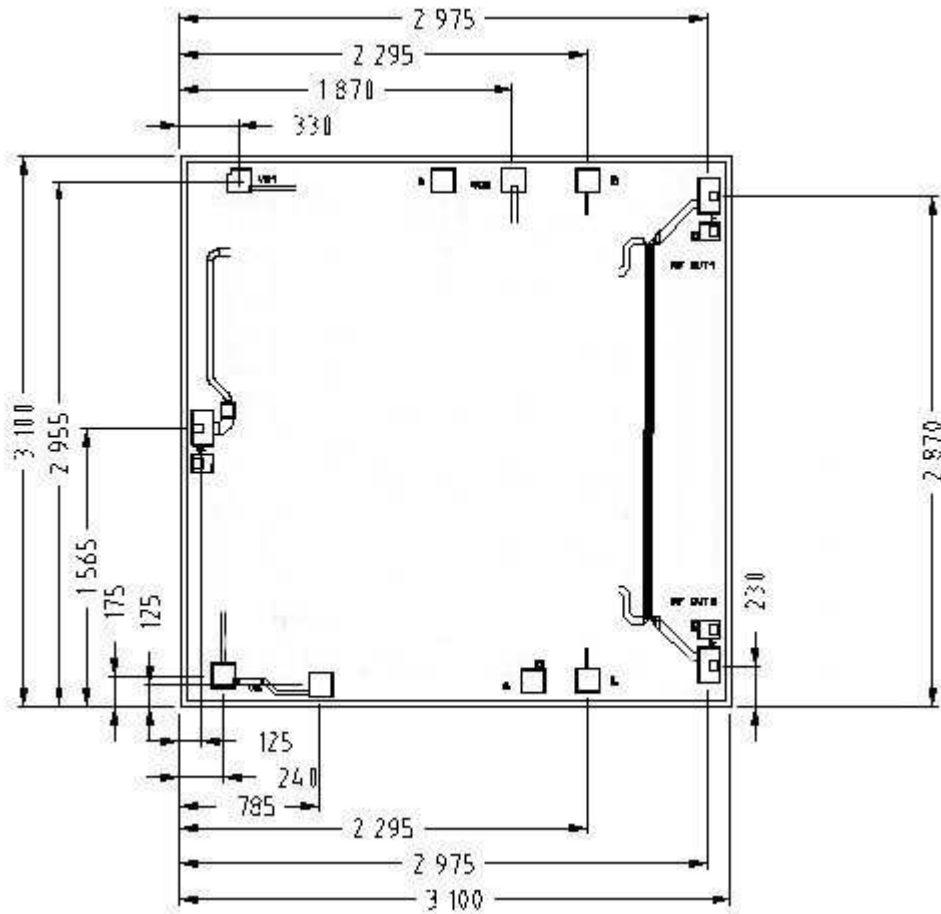
Gain & saturated output power vs frequency in the two SPDT switch configurations



Saturated output power vs temperature in the two SPDT switch configurations

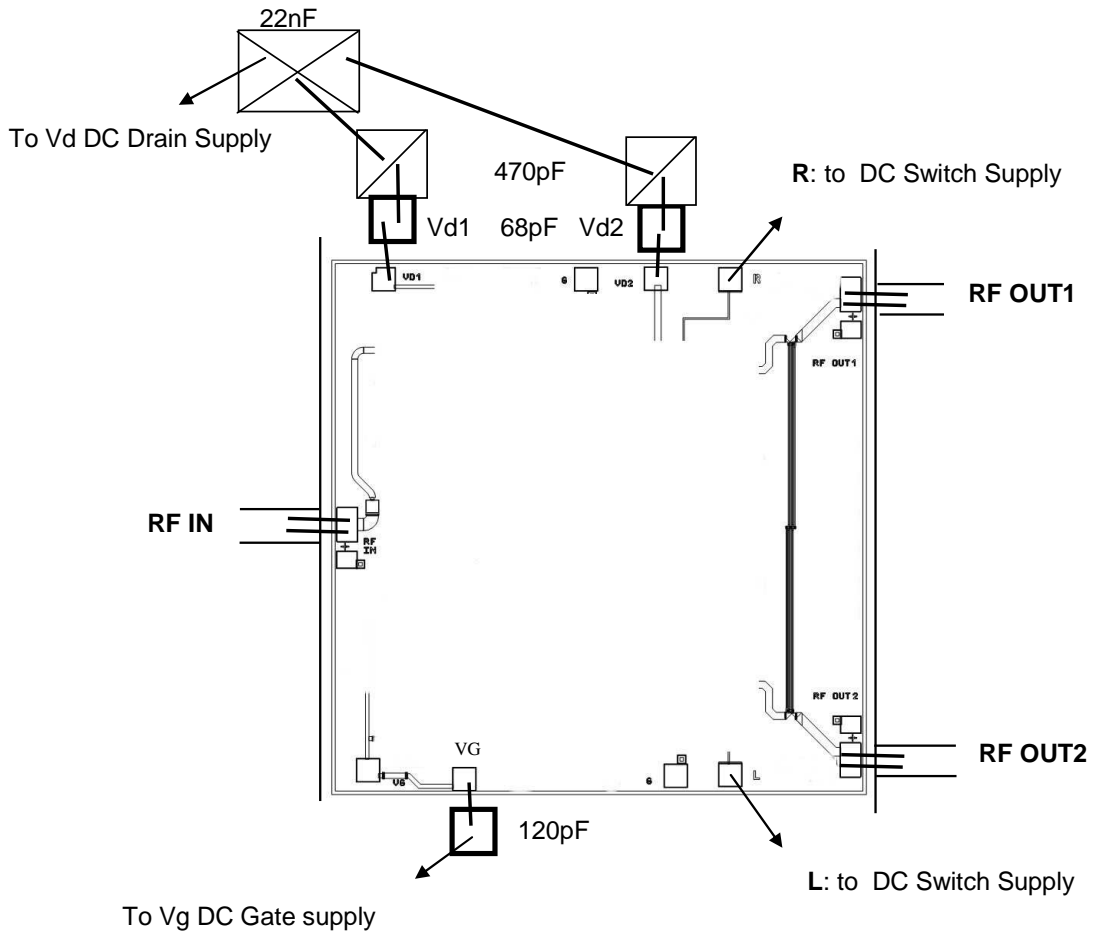


Mechanical data



Chip thickness: 70 μ m.
Chip size: 3100x3100 \pm 35 μ m
All dimensions are in micrometers

Recommended assembly plan



Note: Supply feed should be bypassed. 25µm diameter gold wire is to be preferred.

Recommended circuit bonding table

Label	Type	Decoupling	Comment
R, L	Vc	Not required	SPDT switch pad control
Vd1, Vd2	Vd	68pF & 470pF	Drain Supply
Vg	Vg	120pF	Gate Supply

Notes

Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS products.

Ordering Information

Chip form: CHA3517-99F/XY
Stick: XY = 20 Tape & reel: XY = 21

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