

## 23-26GHz Reflective SP4T Switch

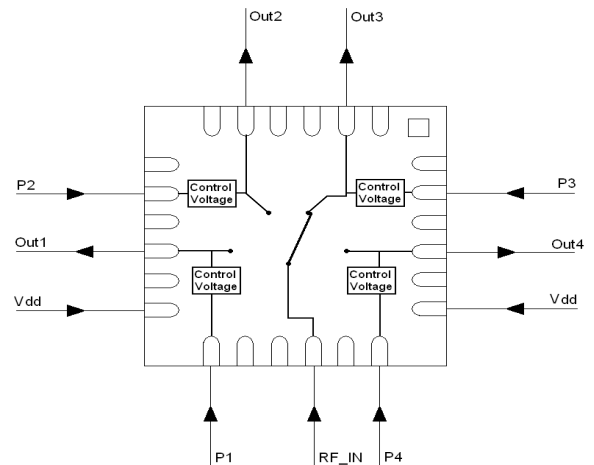
### GaAs Monolithic Microwave IC in QFN package

#### Description

The CHS2411-QDG is a monolithic reflective SP4T switch in K-Band. Positive supply voltage only is required.

The circuit is manufactured with a standard PHEMT process: 0.25 $\mu$ m gate length, via holes through the substrate, air bridges and electron beam gate lithography.

The chip is delivered in a 24 Leads RoHS compliant QFN4x4 package.



*Functional Block Diagram*

#### Main Features

- Low insertion loss : 4 dB max
- High isolation : 32 dB min
- Fast switching time
- Low consumption
- High temperature range
- Positive supply voltage
- 24L-QFN 4x4 SMD Leadless package



*Plastic Package*

#### Main Characteristics

Parameters	Min	Typ	Max	Unit
Frequency range	23		26	GHz
Insertion loss		2.9	4	dB
Isolation	32	35		dB
Return Loss		-15		dB

**ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions !**

## Electrical Characteristics

### Full Temperature Range and nominal state control voltages

Symbol/Pins	Parameters	Min	Typ	Max	Unit
Freq	Frequency range	23		26	GHz
Iso	Isolation	32	35		dB
II	Insertion loss		2.9	4	dB
RI	Return loss		-15		dB
P1dB	Input power at 1 dBc@24GHz	18	23.5		dBm
Ssp	Switching speed		30		ns
Top	Operating temperature range	-40		105	°C

Vdd/5V	Positive Supply Voltage		5		V
Idd/5V	$\Sigma$ of the current on the supply ports (pin6 and 13: see QFN Pin-out description)		3.3	4.3	mA
$\Sigma P_i$ (i=1,2,3,4)	$\Sigma$ of the current on the control ports		3	3.7	mA
Pi (i =1,2,3,4)	OFF state Control Voltage (High state)		5		V
Pi (i =1,2,3,4)	ON state Control Voltage (Low State)		0		V

### Remarks:

- By design the ports OUT1 and OUT2 are respectively symmetrical to ports OUT4 and OUT3.

These performances has been obtained with the chip in QFN package mounted on the recommended boards (ref. 97009 & 97298) described in the document. The performances are highly dependent on this environment.

### For information only:

The main parameters below are obtained from 3 samples mounted on the board ref. 97298 (room temperature).

ON/OFF state Control Voltage	typical			
	Typical insertion loss (dB)	Typical isolation (dB)	Typical return loss (dB)	Typical input power at 1dBc (dBm)
0V/5V	2,9	-35	-15	>22
1V/5V	3.1	-35	-15	16,4
2V/5V	3,7	-35	-15,5	<9
0V/4,5V	3.1	-35.1	-15,4	19,8
0V/4V	3	-35.1	-15,6	22
0,5V/4V	3.1	-35.1	-15,4	17,4
1V/4V	3.1	-35.1	-15	14
2V/4V	no fonctionnal	no funct.	no funct.	no funct.

## Truth Table

Control Pin				Signal Path State			
P1	P2	P3	P4	IN to Out1	IN to Out2	IN to Out3	IN to Out4
<b>Low</b>	High	High	High	<b>ON</b>	OFF	OFF	OFF
High	<b>Low</b>	High	High	OFF	<b>ON</b>	OFF	OFF
High	High	<b>Low</b>	High	OFF	OFF	<b>ON</b>	OFF
High	High	High	<b>Low</b>	OFF	OFF	OFF	<b>ON</b>

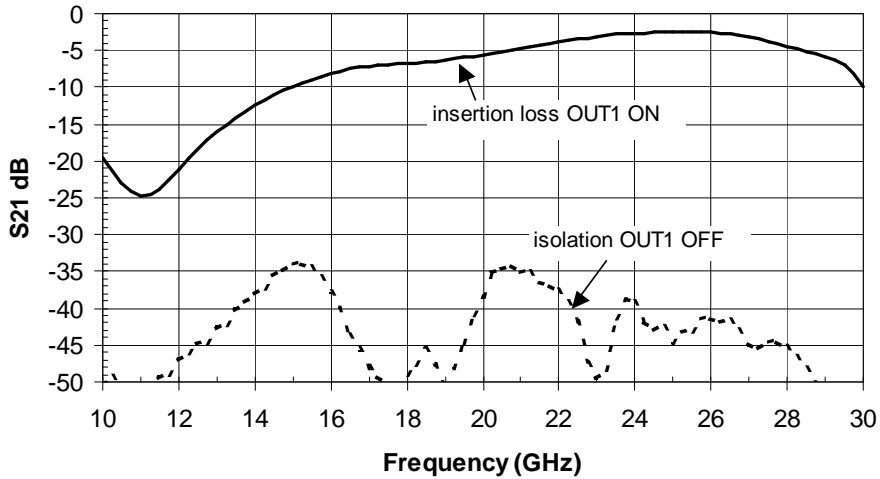
## Absolute Maximum Ratings (1)

Symbol	Parameters	Values	Unit
Vdd	Positive supply voltage	6	V
Pin	Maximum peak input power overdrive	26	dBm
Top	Operating temperature range	-40 to +105	°C
Tstg	Storage temperature range	-55 to +125	°C

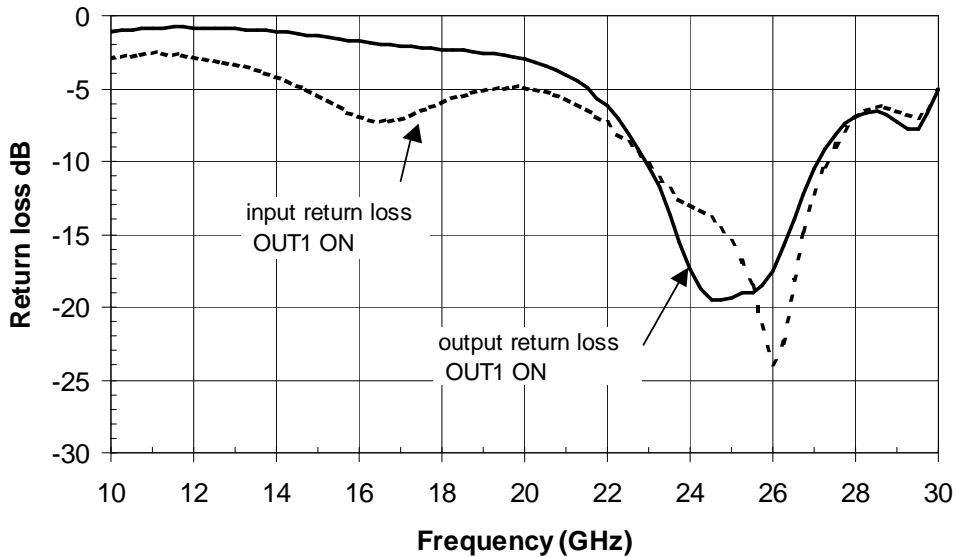
(1) Operation of this device above any one of these parameters may cause permanent damage. Duration < 1s

Typical QFN measurements on board with probes (QFN plan)

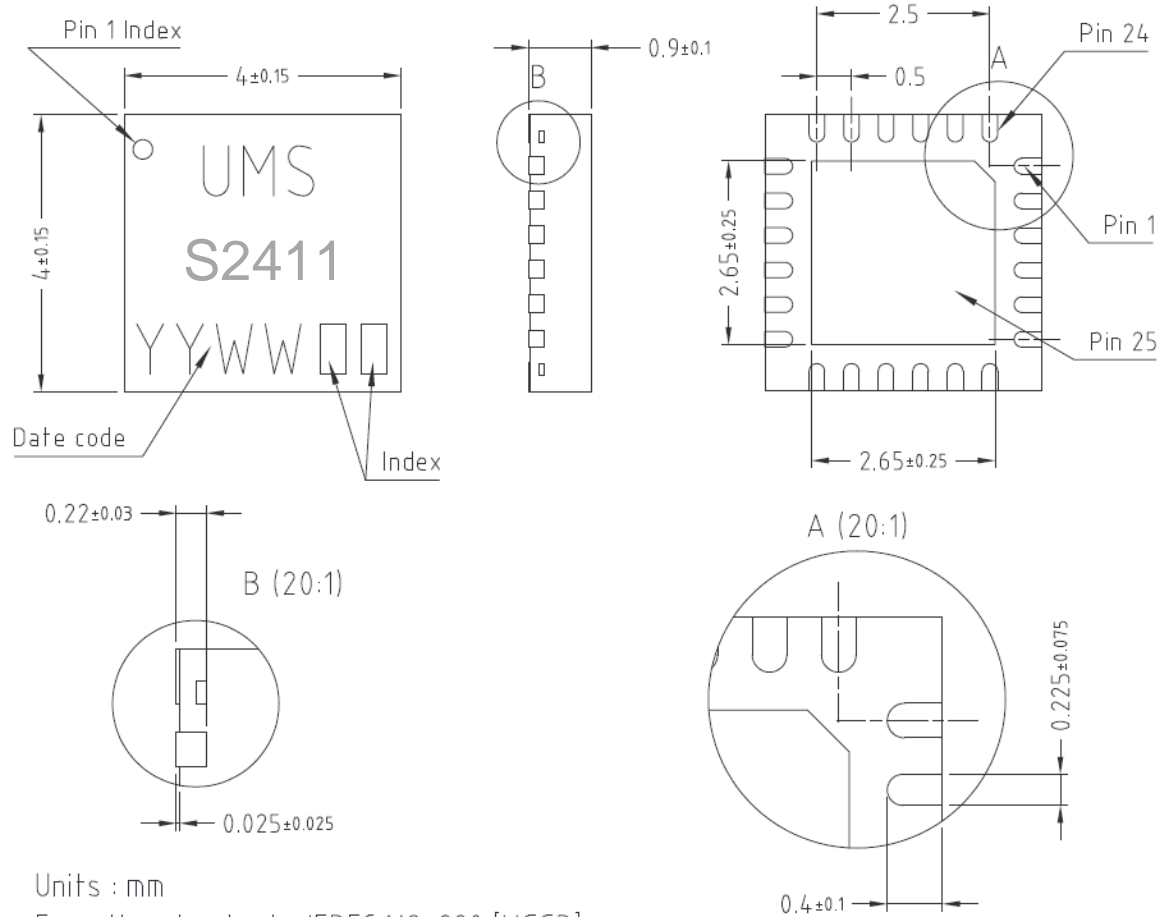
Typical Sij Parameters vs Frequency in QFN package plans  
(RF - OUT1 path)



Typical Sij Parameters vs Frequency in QFN package plans  
(RF - OUT1 path)



**QFN Outlines and Pin-out <sup>(1)</sup>:**



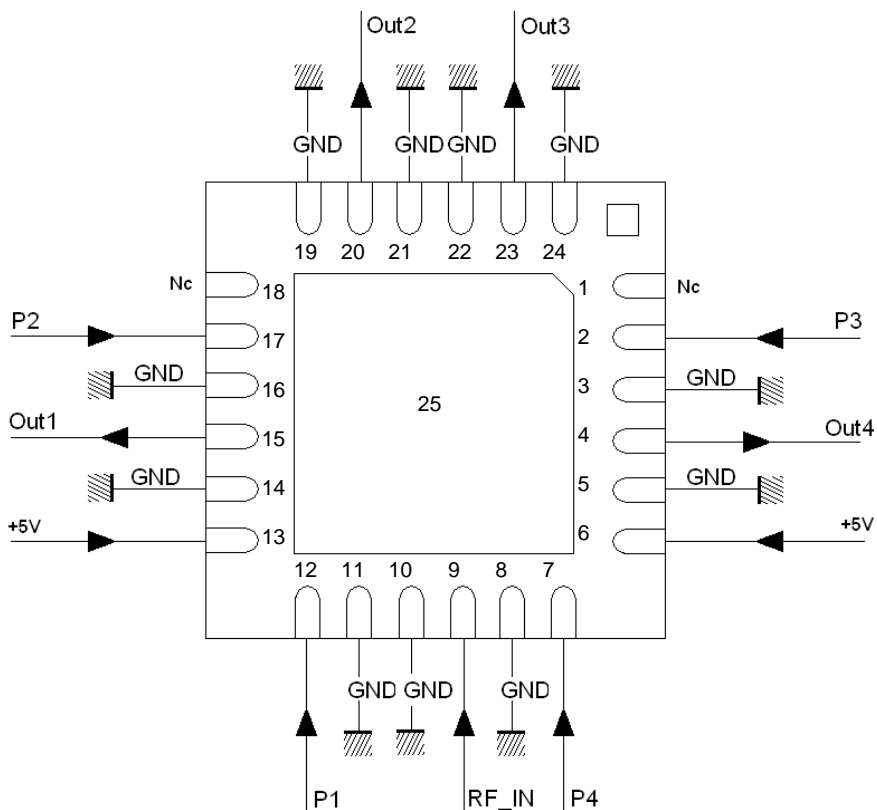
Units : mm  
 From the standard : JEDEC MO-220 [VGGD]  
 Matt tin, Lead free (Green)

<sup>(1)</sup>The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 available at <http://www.ums-gaas.com> for exact package dimensions.

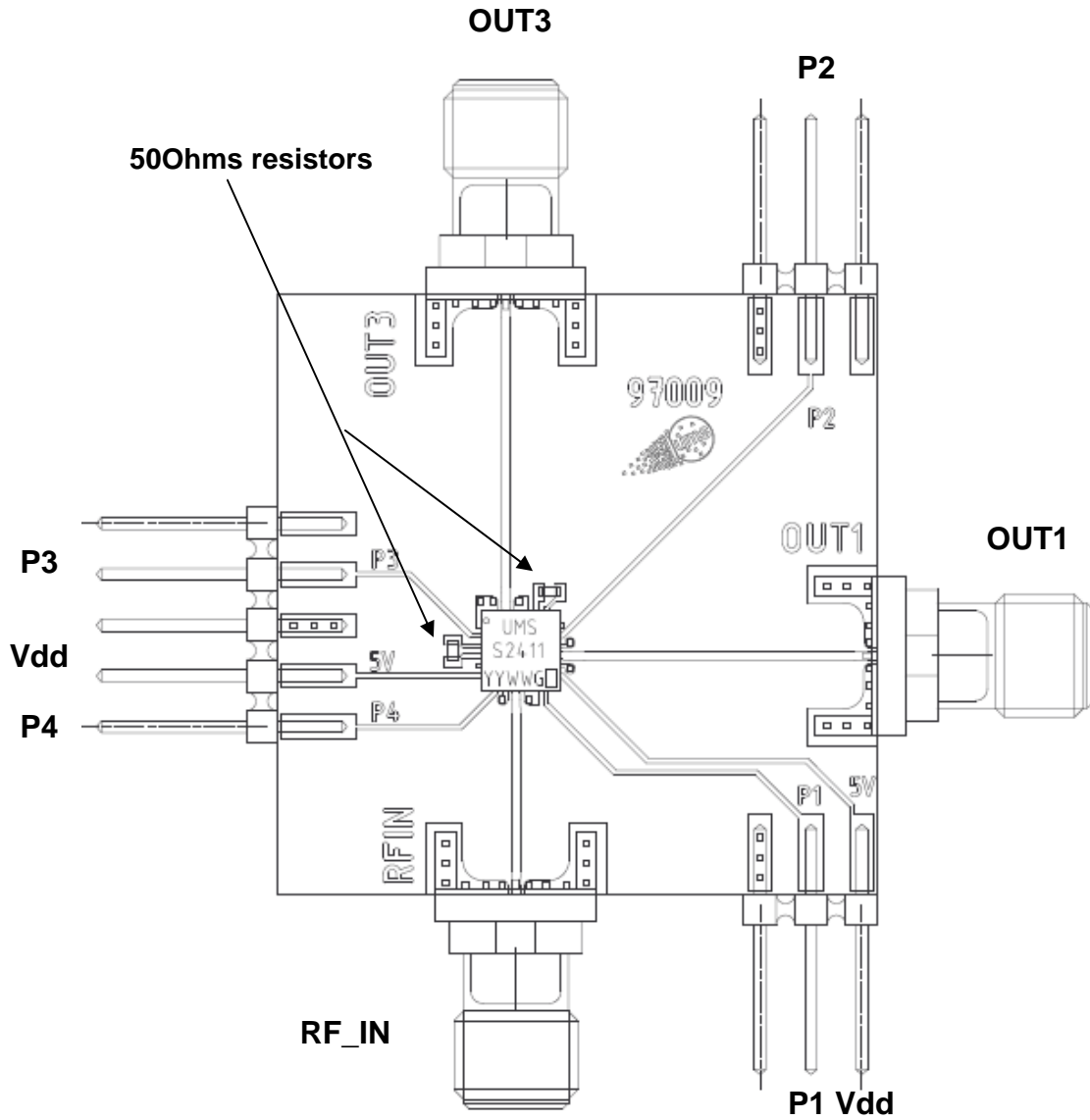
## QFN Pin-out description

Pin number	Pin name	Description
12, 17, 2, 7	P1, P2, P3, P4	Control Voltage port
9, 15, 20, 23, 4	RF IN, Out1, Out2, Out3, Out4	RF1 Input/Output ports
6, 13	5V	Positive supply voltage
3, 5, 8, 10, 11, 14, 16, 19, 21, 22, 24, 25	GND	Ground
1, 18	Nc	Not connected

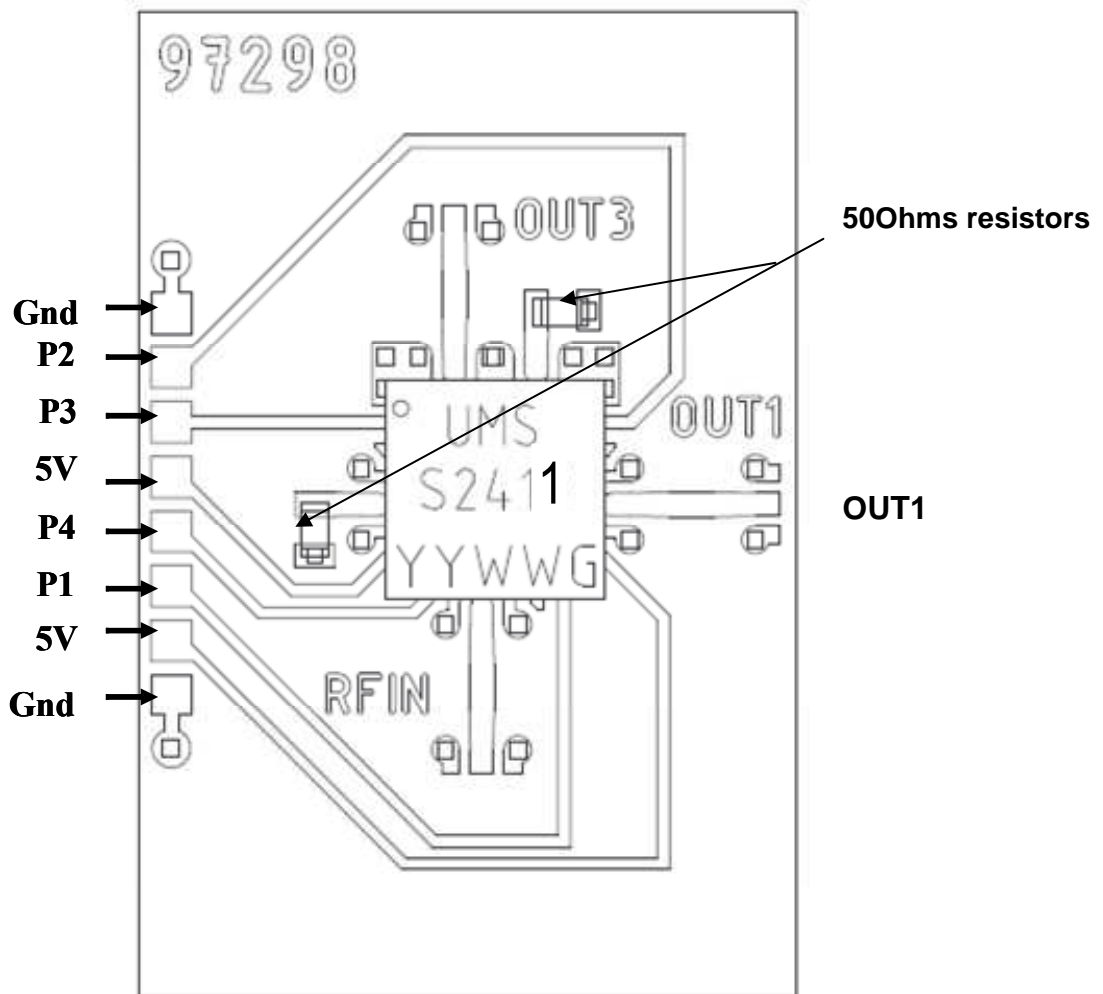
## Bias configuration



Evaluation Test Fixture (Ref. 97009)



**Recommended Test Fixture (Ref. 97298) for measurements in the package's plans with probes**



## ESD sensitivity

Standard	Value
MIL-STD-1686C	HBM Class 1 (<2000V)
ESD STM5.1-1998	HBM Class 0 (<250V)

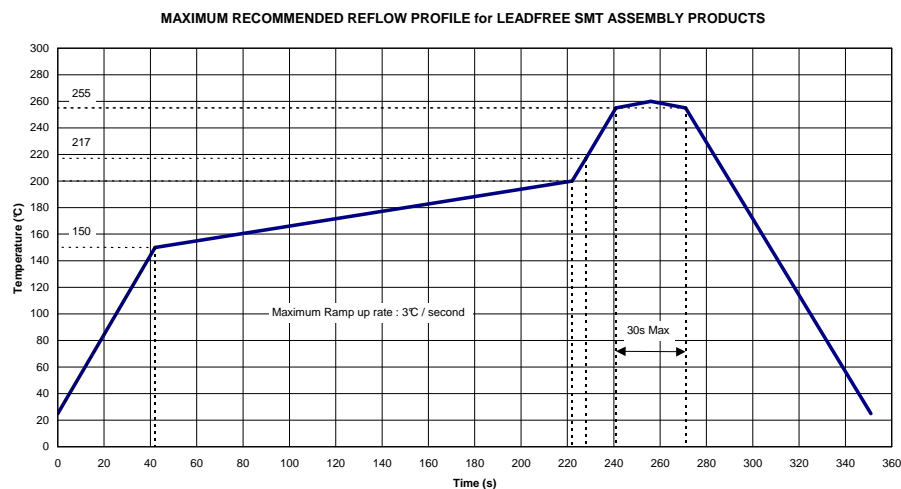
## Package Information

Parameter	Value
Package body material	RoHS-compliant Low stress Injection Molded Plastic
Lead finish	100% matte Sn
MSL Rating	MSL1

## Recommended surface mount package assembly

(See UMS Application note ref. AN0017)

For volume production the SMD type package can be treated as a standard surface mount component (please refer to the IPC/JEDEC J-STD-020C standard or equivalent). The assembly on the motherboard can be performed using a standard assembly process (e.g. stencil solder printing, standard pick-and-place machinery, and solder reflow oven). However, caution should be taken to perform a good and reliable contact over the whole pad area.



The solder thickness after reflow should be typical 50µm [2 mils] and the lateral alignment between the package and the motherboard should be within 50µm [2 mils].

It is important for the performance of the product that the whole overlapping area between the motherboard and package pads is connected. Voids or other improper connections, in particular, between the ground pads on motherboard and package will lead to a deterioration of the RF performance and the heat dissipation. The latter effect can reduce drastically reliability and lifetime of the product.

## Ordering Information

QFN 4x4 RoHS compliant package: CHS2411-QDG/XY

Stick: XY=20            Tape and reel: XY=21

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