

# 17-27GHz Up Converter *Preliminary*

## GaAs Monolithic Microwave IC in SMD package

### Description

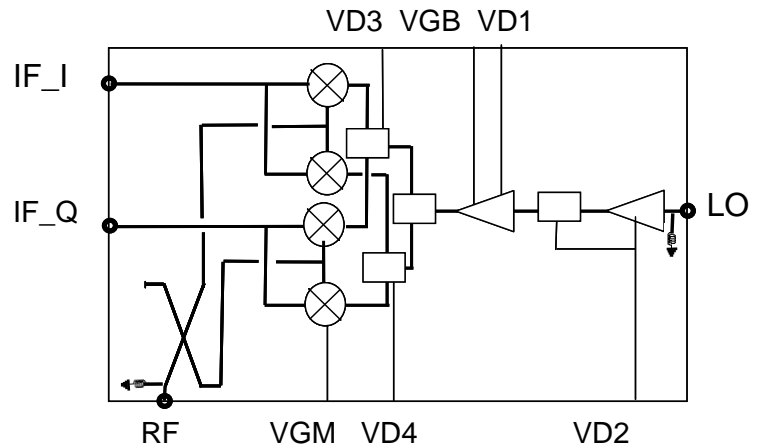
The P015181-QEG is a I/Q up converter, which integrates a balanced cold FET mixer, and a time two multiplier. It is designed for a wide range of applications, typically commercial communication systems.

The circuit is manufactured with a Power pHEMT process, 0.15 $\mu$ m gate length.



### Main Features

- Broadband RF performance 17-27GHz
- 12dB conversion loss
- 24dBm Input IP3
- 15dB Image rejection
- 24LQFN4x5
- ESD protected (see page 12)



### Main Characteristics

Tamb = +25°C, Vd= 5V

Symbol	Parameter	Min	Typ	Max	Unit
F <sub>RF</sub>	RF frequency range	17		27	GHz
F <sub>LO</sub>	LO frequency range	7.5		14.75	GHz
F <sub>IF</sub>	IF frequency range	0.5		2.5	GHz
L <sub>c</sub>	Conversion Loss		12		dB

ESD Protections: Electrostatic discharge sensitive device observe handling precautions!

## Electrical Characteristics

**Preliminary**T<sub>amb</sub> = +25°C, V<sub>d</sub> = 5V

Symbol	Parameter	Min	Typ	Max	Unit
F <sub>RF</sub>	RF frequency range	17		27	GHz
F <sub>LO</sub>	LO frequency range	7.5		14.75	GHz
F <sub>IF</sub>	IF frequency range	0.5		2.5	GHz
L <sub>c</sub>	Conversion loss		-12		dB
P <sub>LO</sub>	LO Input power		5		dBm
IIP3	Input IP3		24		dBm
Im Rej	Image Rejection		15		dBc
LO RL	LO Return Loss		-10		dB
IF RL	IF Return Loss		-8		dB
2LO/RF	2LO leakage at RF port		-25		dBm
VD <sub>x</sub>	DC drain voltage		5		V
I <sub>d</sub>	Drain current		260		mA
V <sub>GM</sub>	DC gate voltage		-5		V
V <sub>GB</sub>	DC gate voltage		-5		V

*These values are representative of onboard measurements as defined on the drawing at page 13 (paragraph "Evaluation mother board").*

**Absolute Maximum Ratings** <sup>(1)</sup>T<sub>amb</sub> = +25°C**Preliminary**

Symbol	Parameter	Values	Unit
VD <sub>x</sub>	Maximum drain bias voltage (VD1, VD2, VD3, VD4)	5.5	V
I <sub>d</sub>	Maximum drain bias current	400	mA
VGM, VGB	Maximum gate bias voltage	-6	V
P <sub>IF</sub>	Maximum peak input power overdrive	20	dBm
P <sub>LO</sub>	Maximum LO input power	10	dBm
T <sub>ch</sub>	Maximum channel temperature	175	°C
T <sub>a</sub>	Operating temperature range	-40 to +80	°C
T <sub>stg</sub>	Storage temperature range	-55 to +125	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

*Preliminary*

**Device thermal performances**

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered).

The temperature is monitored at the package back-side interface (Tcase) as shown below. The system maximum temperature must be adjusted in order to guarantee that Tcase remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

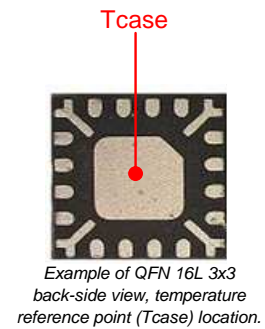
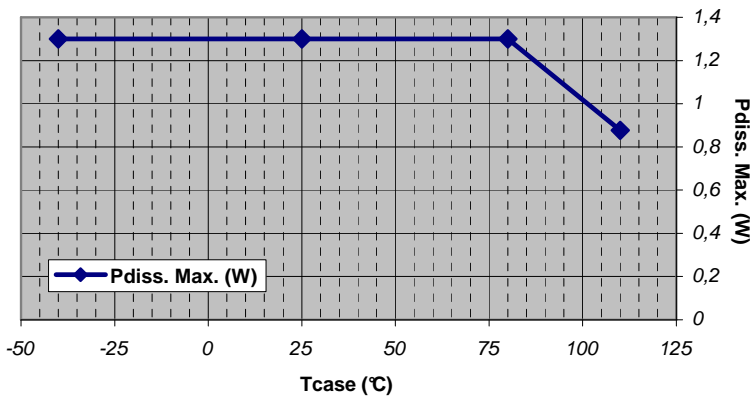
A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below than the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

DEVICE THERMAL SPECIFICATION : PO15181		
Max. junction temperature (Tj max)	:	172 °C
Max. continuous dissipated power @ Tcase= 80 °C	:	1,3 W
=> Pdiss derating above Tcase <sup>(1)</sup> = 80 °C	:	14 mW/°C
Junction-Case thermal resistance (Rth J-C) <sup>(2)</sup>	:	<70 °C/W
Min. package back side operating temperature <sup>(3)</sup>	:	-40 °C
Max. package back side operating temperature <sup>(3)</sup>	:	80 °C
Min. storage temperature	:	-55 °C
Max. storage temperature	:	125 °C

(1) Derating at junction temperature constant = Tj max.

(2) Rth J-C is calculated for a worst case where the **hotter junction** of the MMIC is considered.

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).



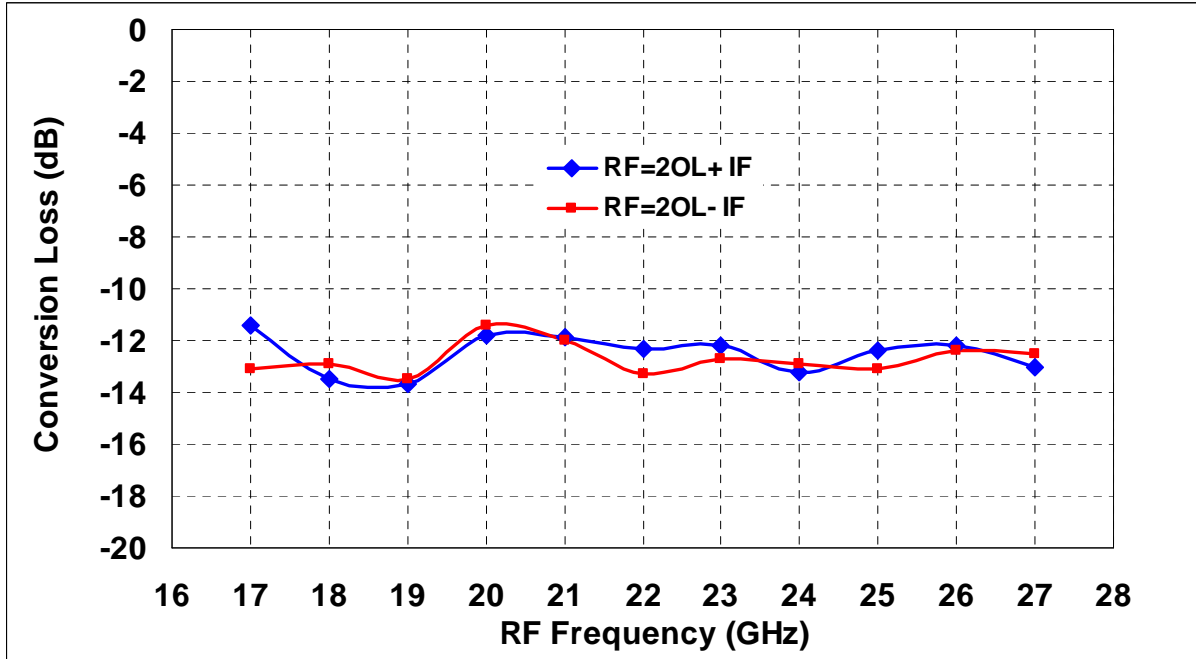
Typical Measured Performances

*Preliminary*

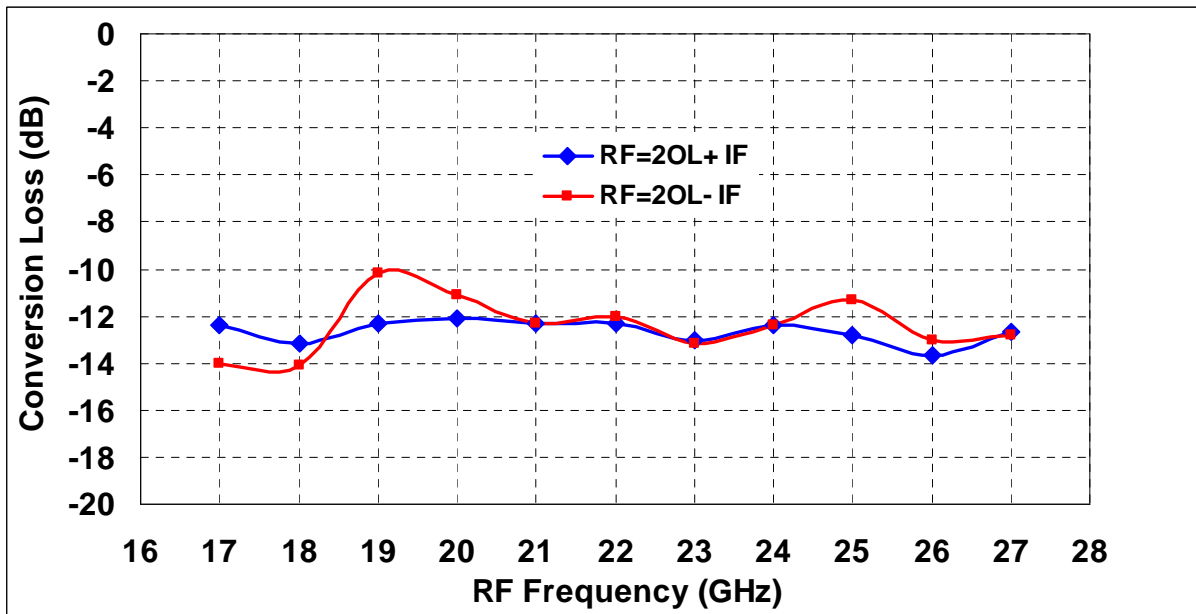
Tamb= +25°C, VD= 5V, VGB= -5V, VGM= -5V, P\_LO= 5dBm

These values are representative of onboard measurements (on connector access planes) as defined on the drawing 97639 page 13. The board loss is estimated to 1.5 to 2dB in the frequency range.

Conversion loss with IF= 1GHz & -20dBm



Conversion loss with IF= 2GHz & -20dBm



Conversion loss with IF= 2GHz& RF=2LO+ IF  
Versus temperature

*Preliminary*

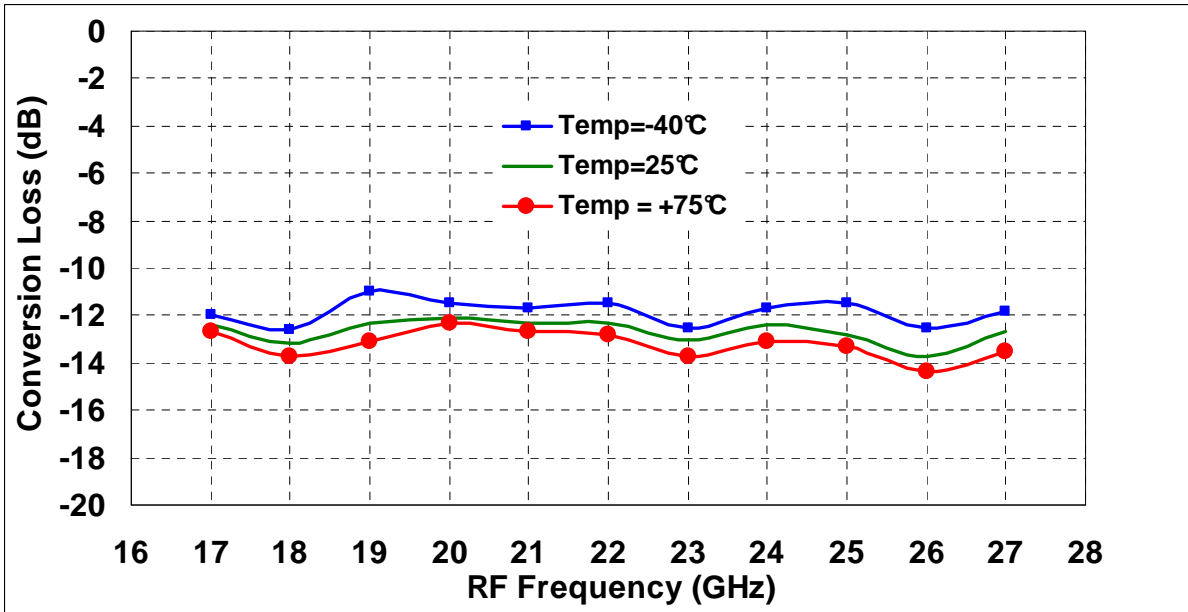
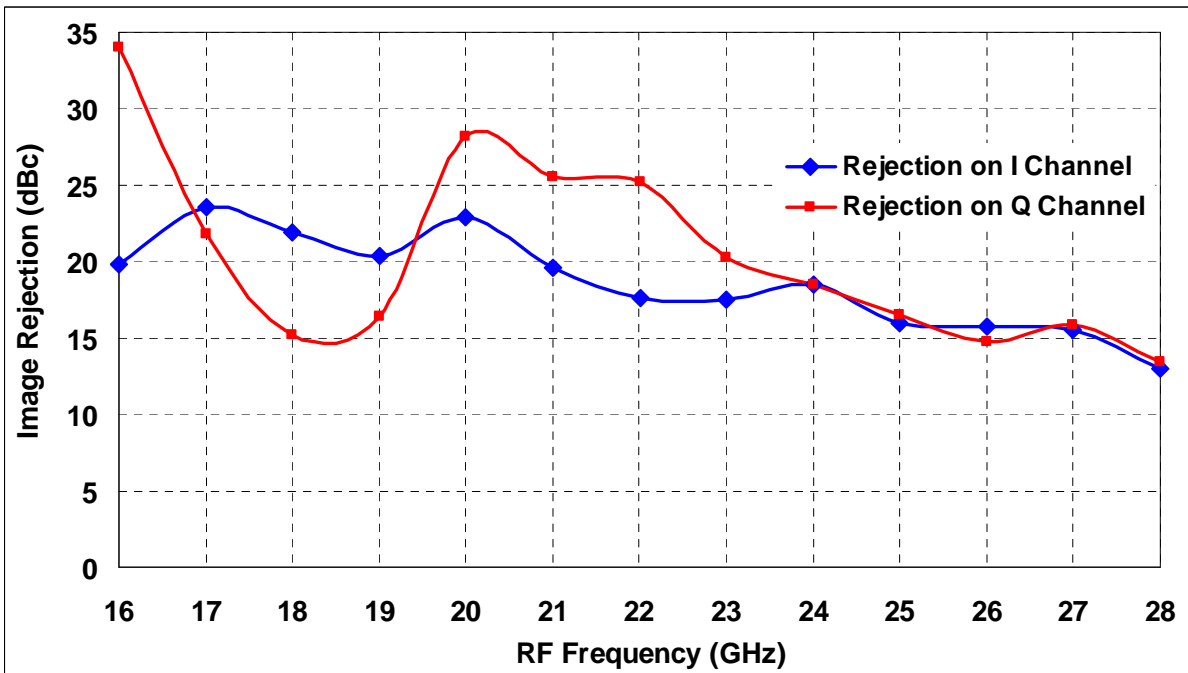
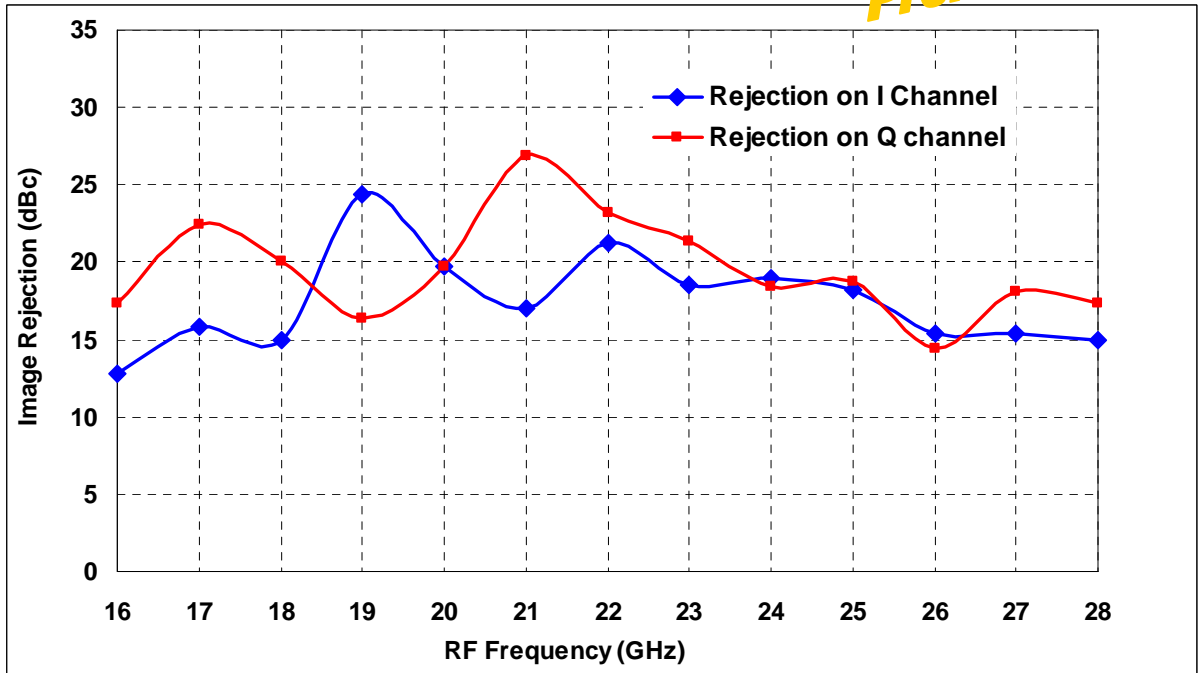


Image rejection with IF= 1GHz

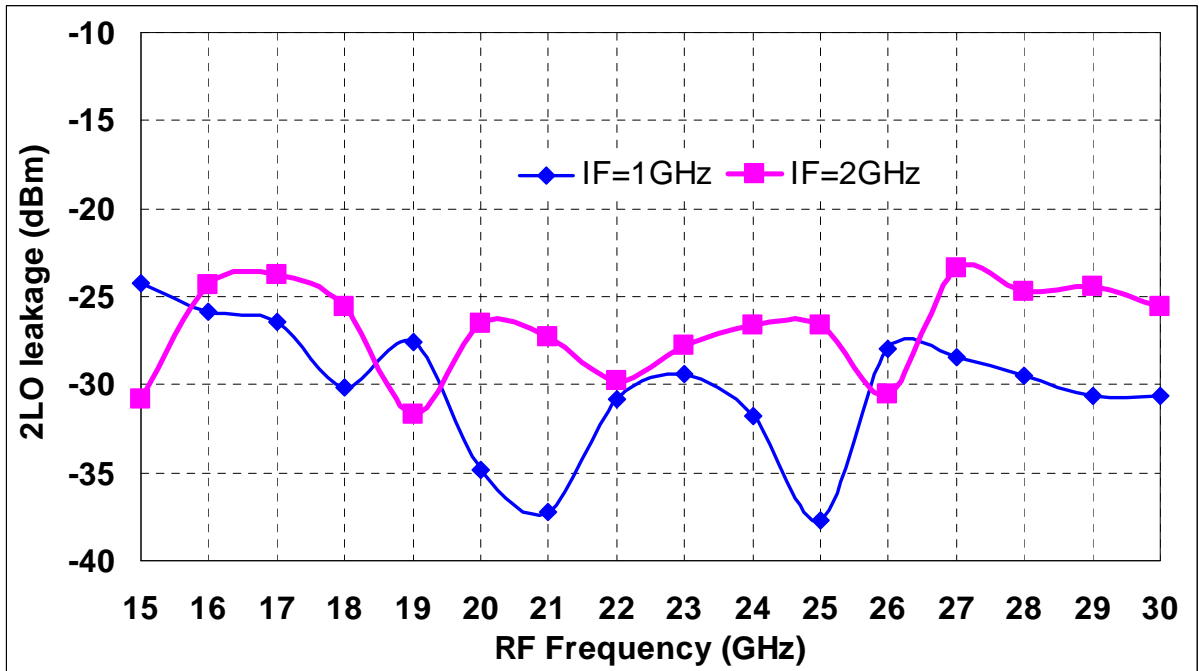


*Preliminary*

Image rejection with IF= 2GHz

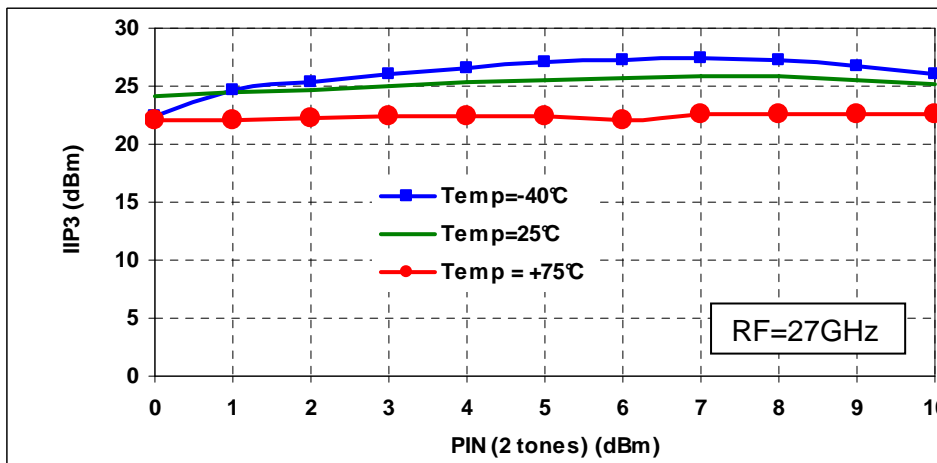
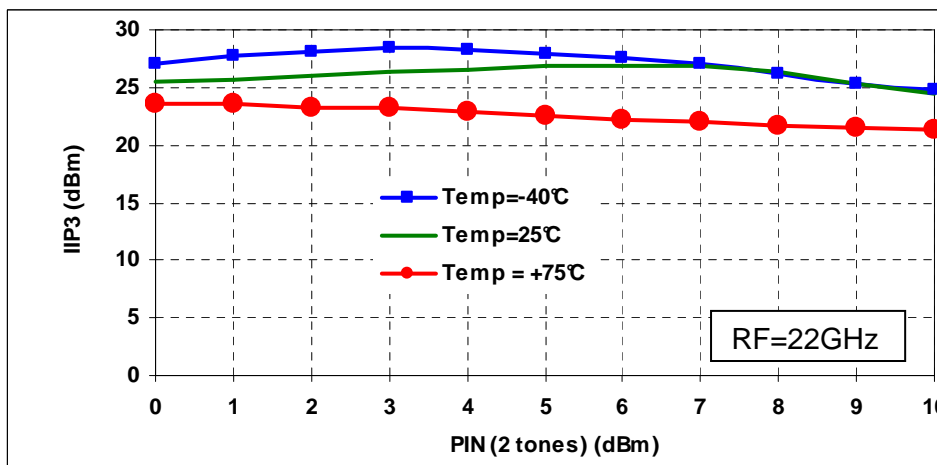
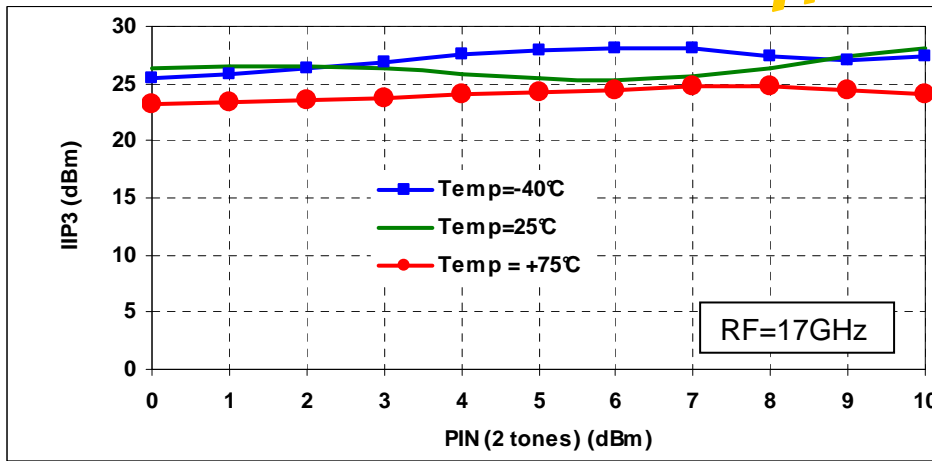


2LO leakage on RFchannel @ P\_LO=5dBm



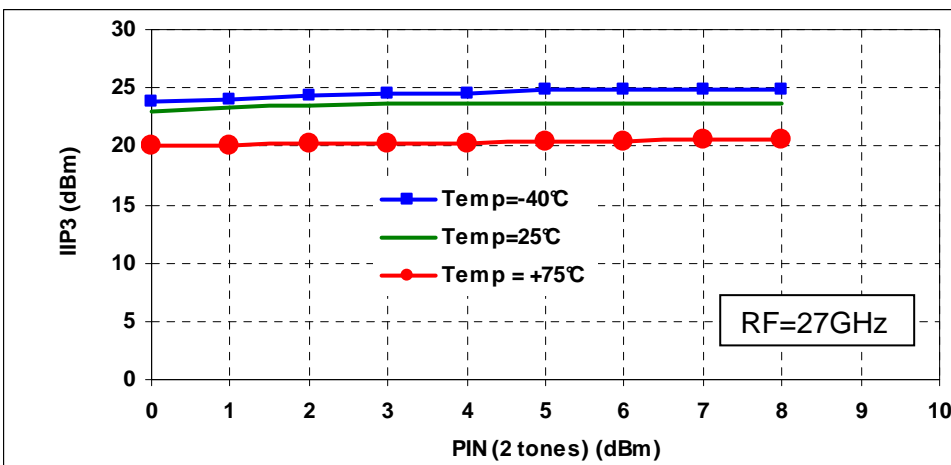
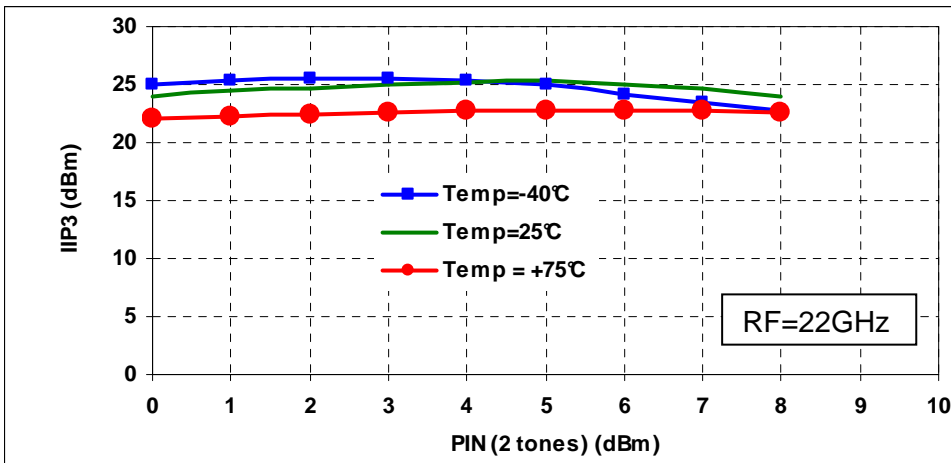
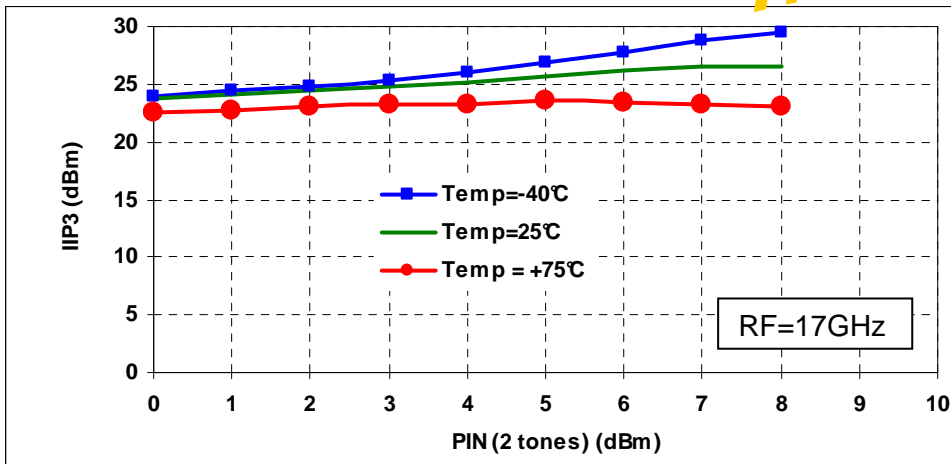
*Preliminary*

Input IP3@ IF= 1GHz, RF= 2LO- IF

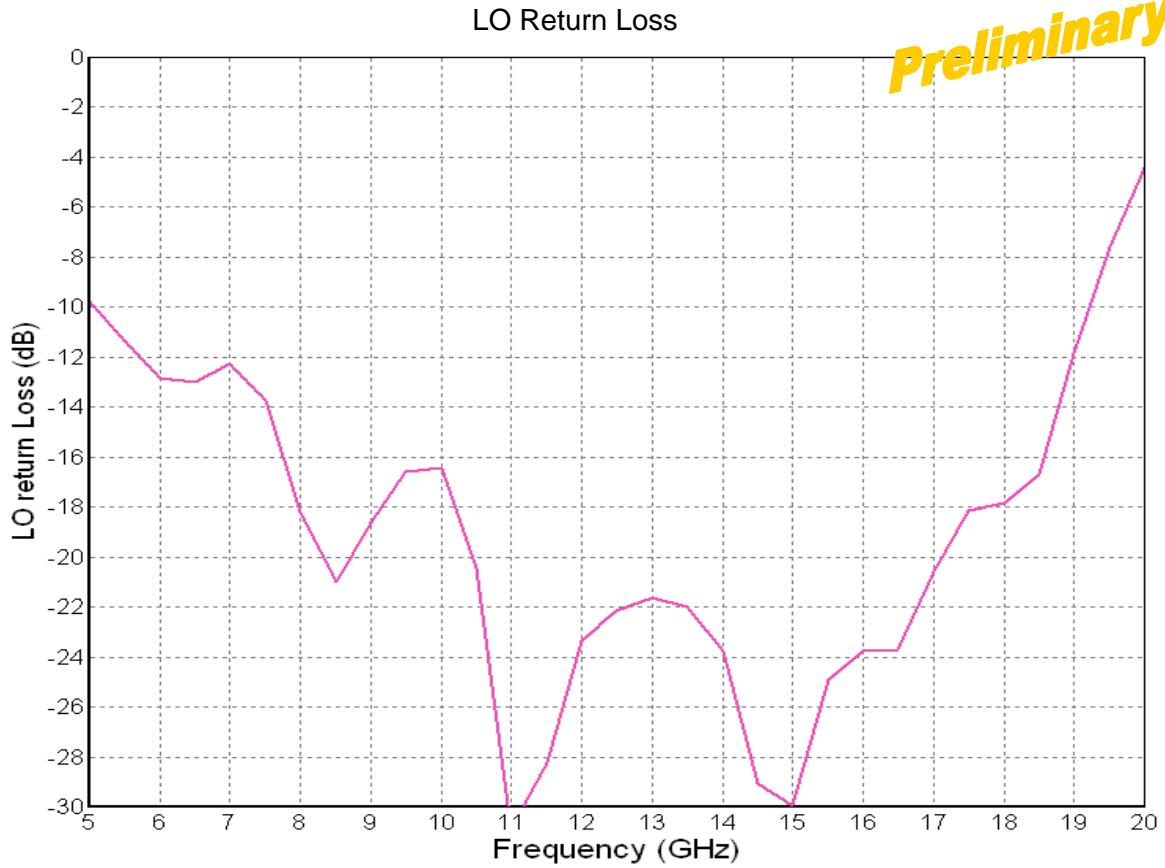


*Preliminary*

Input IP3@ IF= 2GHz, RF= 2LO- IF

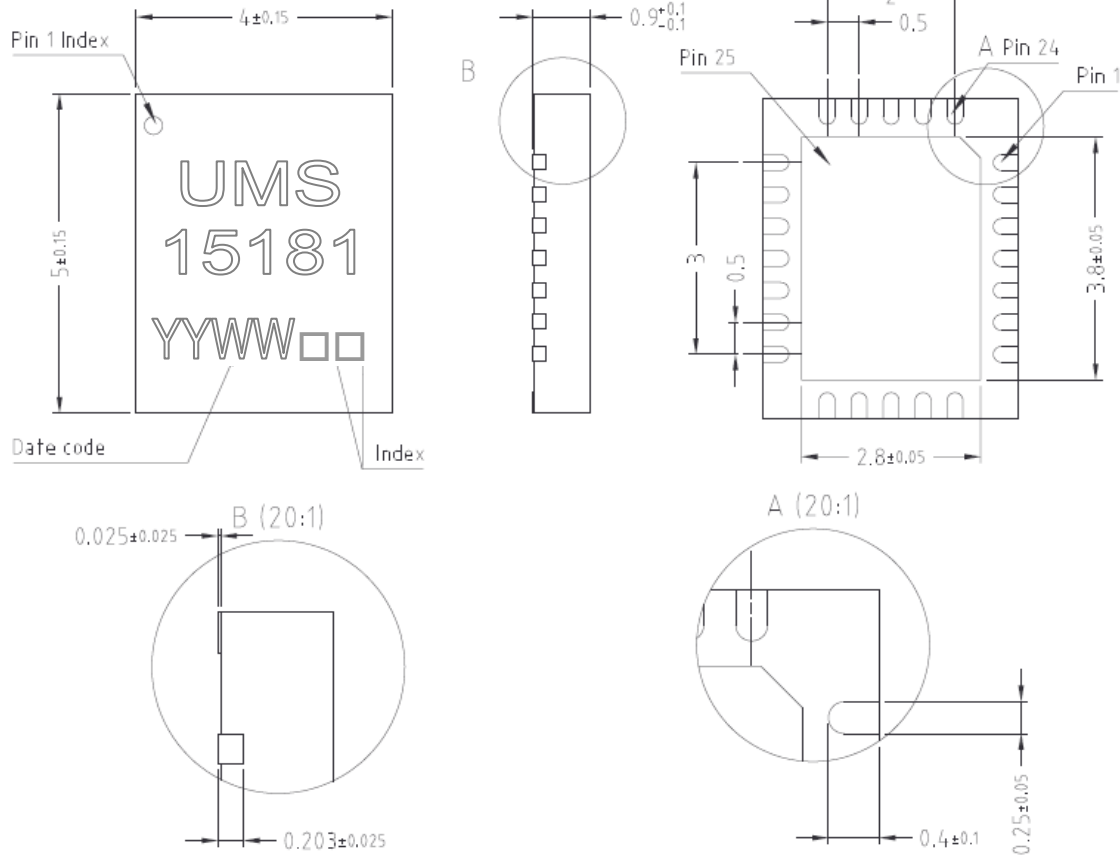


*Preliminary*



**Preliminary**

**Package outline (1)**



Units : mm

From the standard : JEDEC MO-220 [ VGHD]

Matt tin, Lead free (Green)

1- Nc	9- RF	17- VGB	25- GND Exposed Pad
2- Nc	10- Gnd	18- VD1	
3- VD2	11- Nc	19- Gnd	
4- VD4	12- Nc	20- Nc	
5- VGM	13- IF-I	21- Nc	
6- Gnd	14- Gnd	22- Gnd	
7- IF-Q	15- VGM	23- LO	
8- Gnd	16- VD3	24- Gnd	

(1)The package outline drawing included to this data-sheet is given for indication. Refere to the application note AN0017 available at <http://www.ums-gaas.com> for exact package dimensions.

(2)It is strongly recommended to ground all the pins Gnd on the PCB board.

*Preliminary*

**Recommended package footprint**

Refer to the application note AN0017 available at <http://www.ums-gaas.com> for package footprint recommendations.

**SMD mounting procedure**

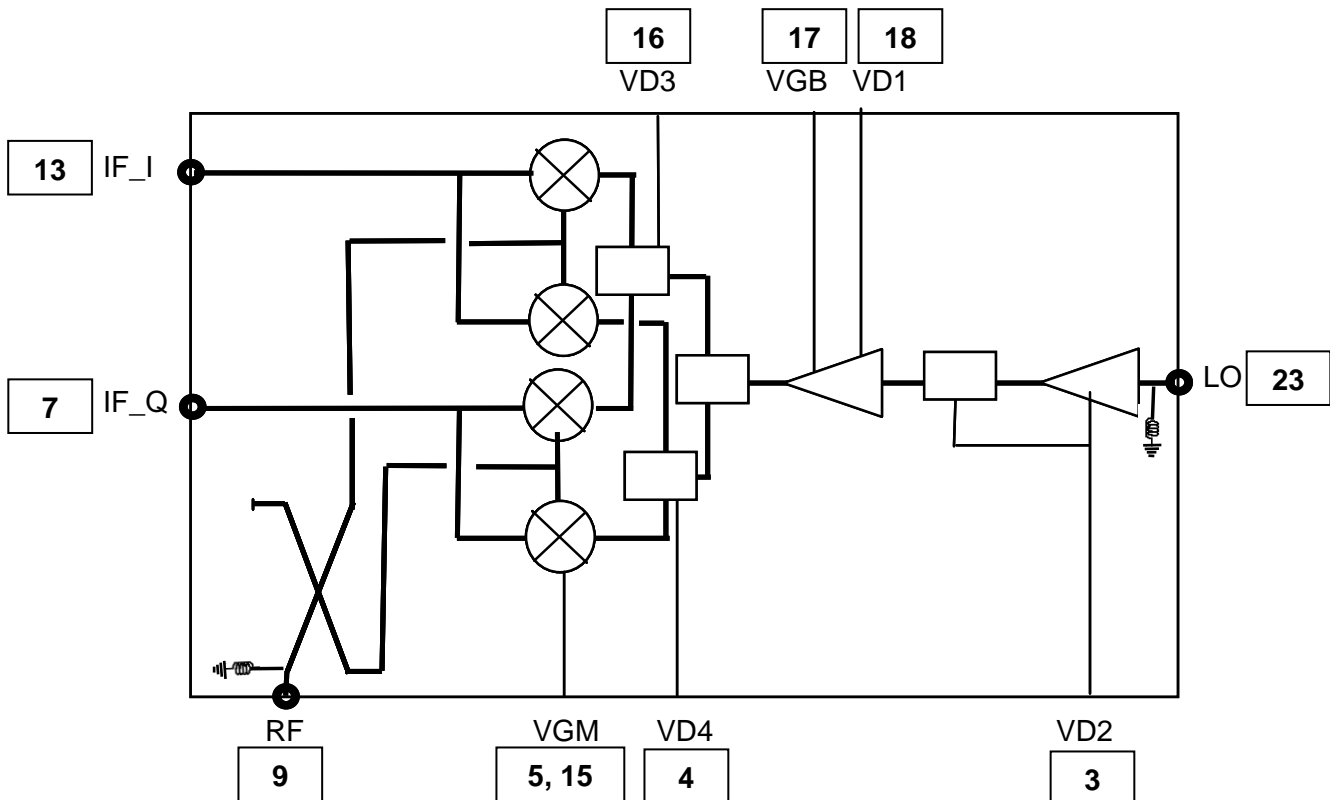
The SMD leadless package has been designed for high volume surface mount PCB assembly process. The dimensions and footprint required for the PCB (motherboard) are given in the drawings above.

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

**Notes**

Due to ESD protection circuits on RF output and LO input, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.

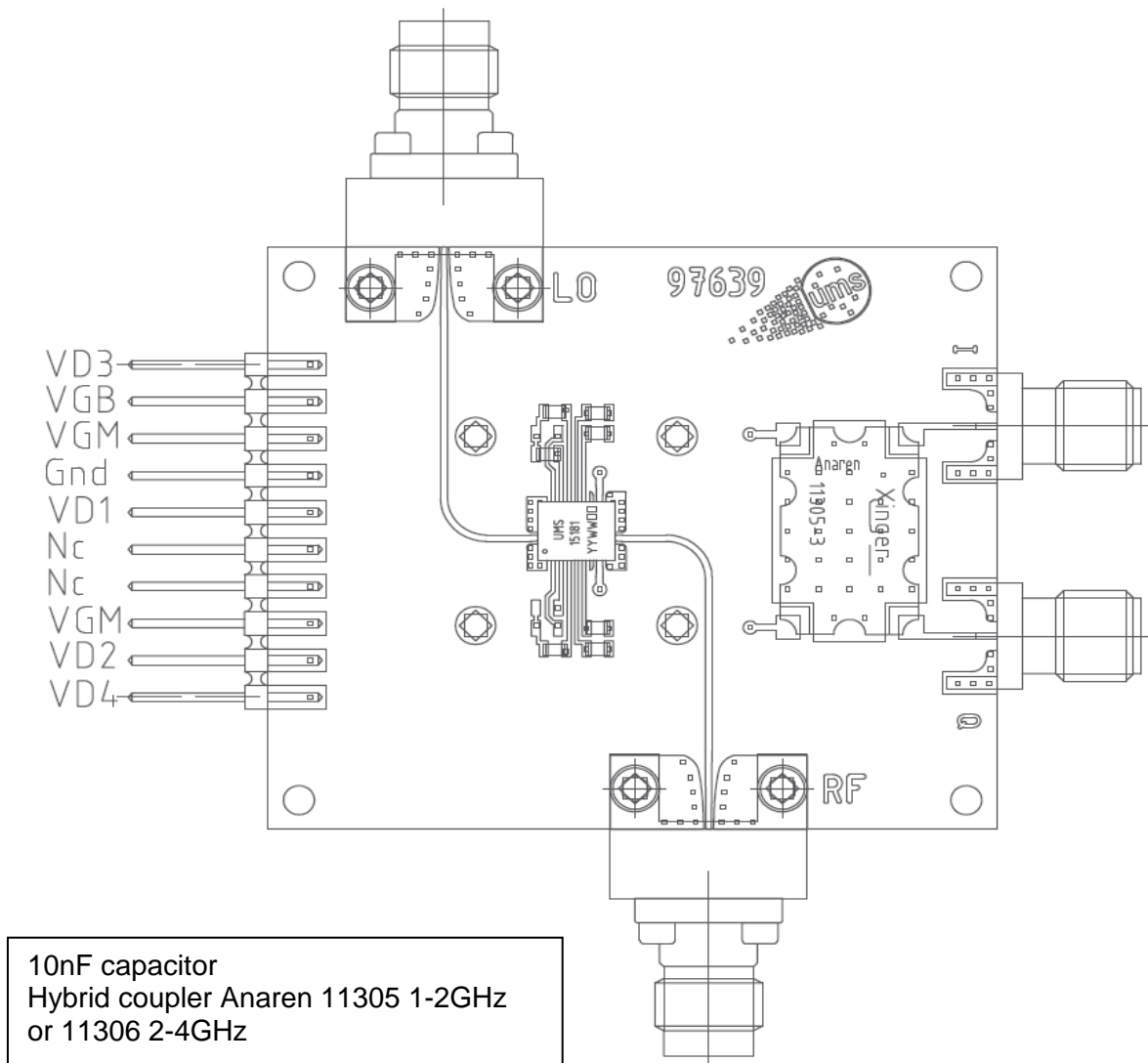
ESD protections are also implemented on gate accesses.



## Evaluation mother board

**Preliminary**

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a microstrip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF  $\pm 10\%$  are recommended for all DC accesses.
- (See application note AN0017 for details).



## Ordering Information

QFN 4x5 RoHS compliant package: MFC-PO15181-QEG/XY  
Stick: XY = 20      Tape & reel: XY = 21

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