

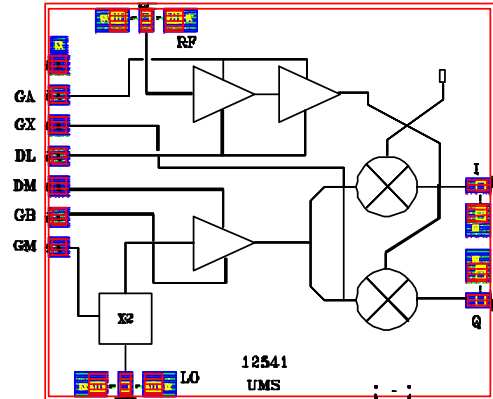
12-16GHz Integrated Down Converter

GaAs Monolithic Microwave IC

Description

The CHR2391 is a multifunction chip which integrates a LO time two multiplier, a balanced cold FET mixer, and a RF LNA. It is designed for a wide range of applications, typically commercial communication systems. The backside of the chip is both RF and DC grounds. This helps to simplify the assembly process.

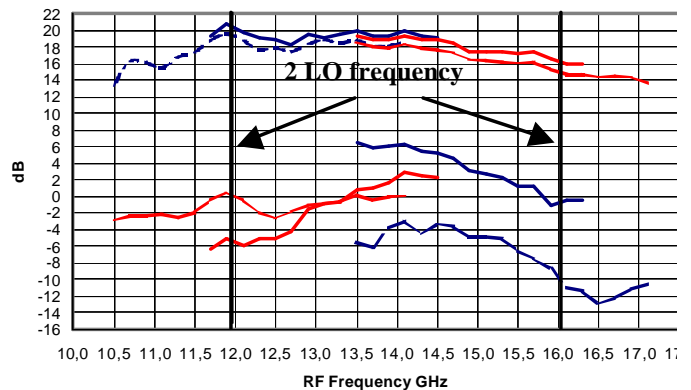
The circuit is manufactured with a PM-HEMT process, 0.25µm gate length, via holes through the substrate and air bridges. It is available in chip form.



Main Features

- Broadband performances : 12.0-16.0GHz
- 15 dB conversion gain
- 2dB noise figure
- 10dBm LO input power
- -10dBm RF input power (1dB gain comp.)
- Low DC power consumption, 100mA@3.5V
- Chip size : 2.49 X 2.13 X 0.10 mm

Typical on wafer measurement:
Conversion Gain & Image suppression
@ IF=0.9 & 1.5GHz



Main Characteristics

Tamb. = 25°C

	Parameter	Min	Typ	Max	Unit
F_{RF}	RF frequency range	12		16	GHz
F_{LO}	LO frequency range	5.25		7.25	GHz
F_{IF}	IF frequency range	0.25		1.5	GHz
G_c	Conversion gain	13	+15		dB

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

Ref. : DSCHR23915263 - 20 Sep 05

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Specifications subject to change without notice

Electrical Characteristics for Broadband OperationT_{amb} = +25°C, V_d = 3.5V, |I_d|=50mA, I_{dm}=50mA

Symbol	Parameter	Min	Typ	Max	Unit
F _{RF}	RF frequency range	12		16	GHz
F _{LO}	LO frequency range	5.25		7.25	GHz
F _{IF}	IF frequency range	0.25		1.5	GHz
G _c	Conversion gain (1)	+13	+15		dB
NF	Noise Figure (1)		2.	2.5	dB
P _{LO}	LO Input power		+10	+13	dBm
Img Sup	Image Suppression		15		dBc
P1dB	Input power at 1dB gain compression		-10		dBm
IP3	Input IP3		2.5		dBm
LO VSWR	Input LO VSWR (1)		2.0:1		
RF VSWR	Input RF VSWR (1)		2.0:1		
I _d	Bias current (2)		100	130	mA

(1) On Wafer measurements

(2) Current source biasing network is recommended.

Optimum performances are obtained for I_{dm}=50mA (I_d consumption of the X2+buffer; V_{gb}≠-0.4V) and |I_d|=50mA (I_d consumption for the I_{na}; V_{ga}≠-0.4V)**Absolute Maximum Ratings**T_{amb.} = 25°C (1)

Symbol	Parameter	Values	Unit
V _d	Maximum drain bias voltage	4.0	V
I _d	Maximum drain bias current	180	mA
V _g	Gate bias voltage	-2.0 to +0.4	V
V _{dg}	Maximum drain to gate voltage (V _d – V _g)	+5	V
P _{in}	Maximum RF peak input power overdrive (2)	-5	dBm
T _{ch}	Maximum channel temperature	175	°C
T _a	Operating temperature range	-40 to +85	°C
T _{stg}	Storage temperature range	-55 to +125	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

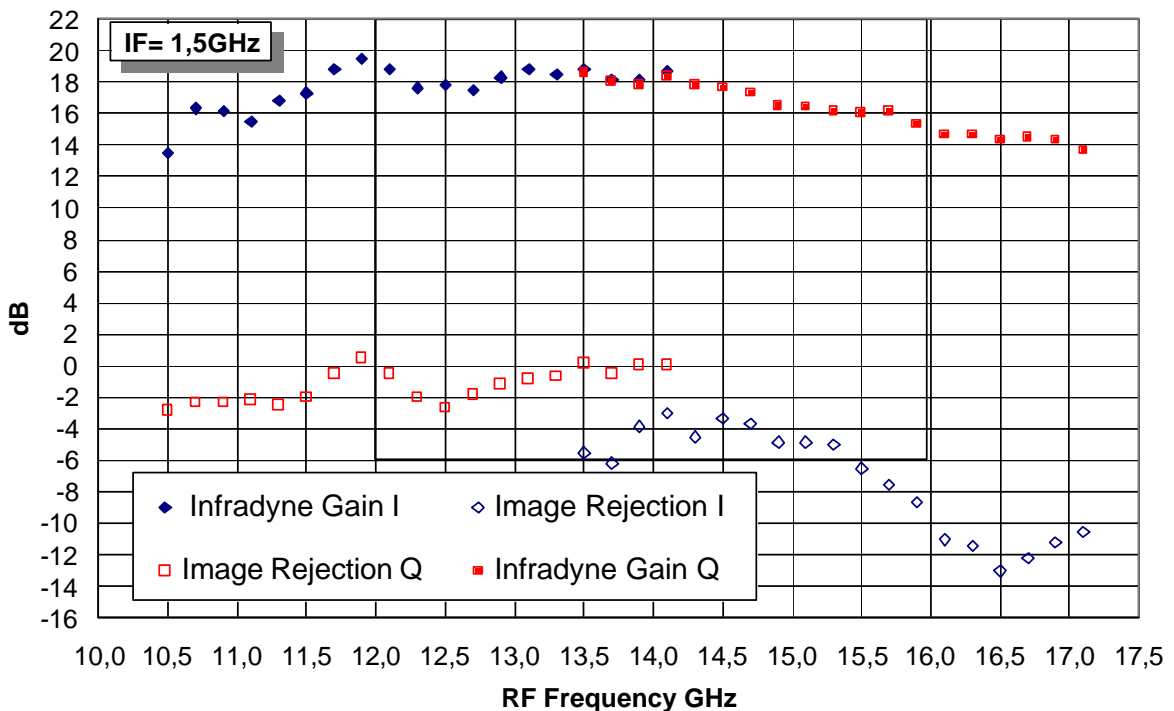
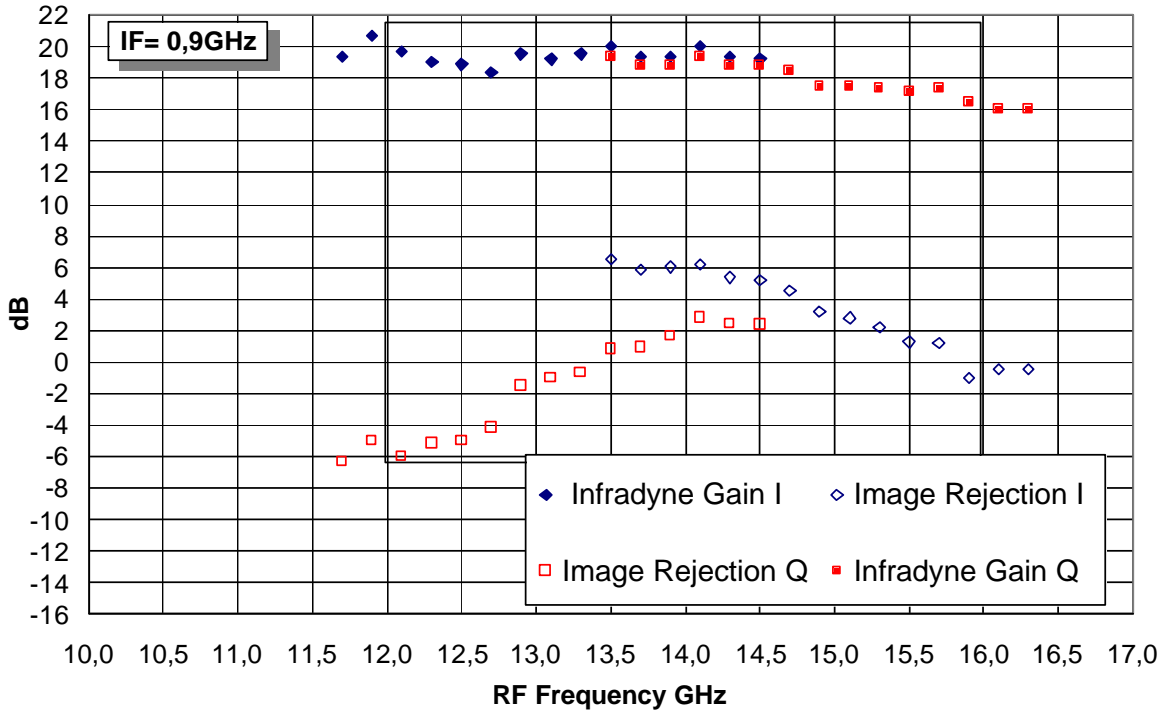
(2) Duration < 1s.

Typical On-wafer Measurements

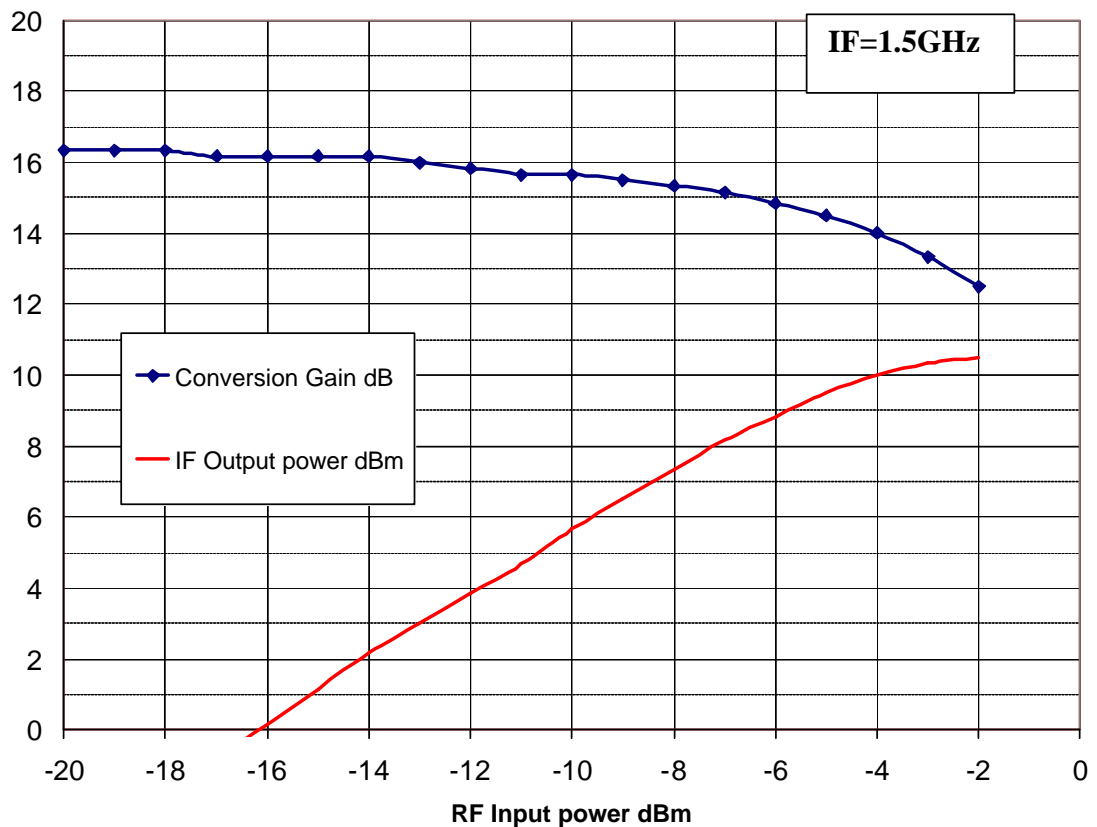
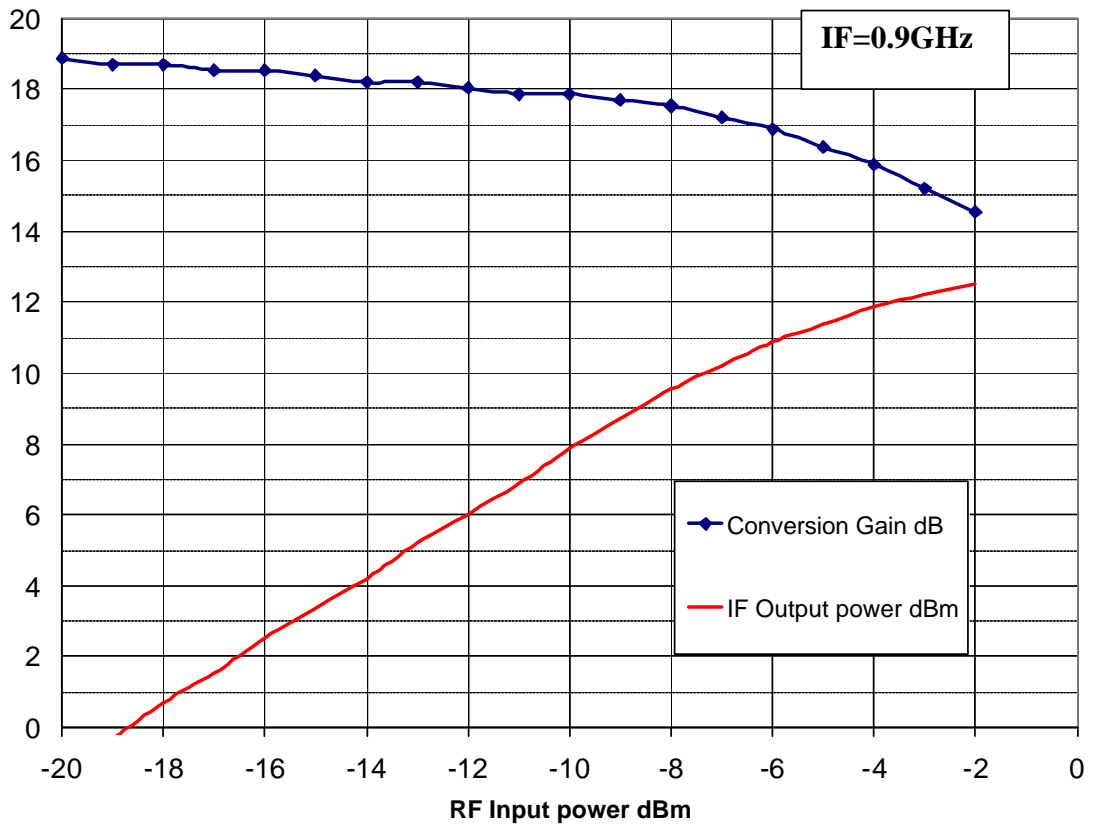
Bias Conditions :

$V_{dm} = V_{dl} = 3.5\text{ V}$, $I_{dl} = I_{dm} = 50\text{mA}$ ($V_{ga} = v_{gb} = -0.4\text{V}$), $V_{gm} = -0.7\text{V}$, $V_{gx} = -0.6\text{V}$

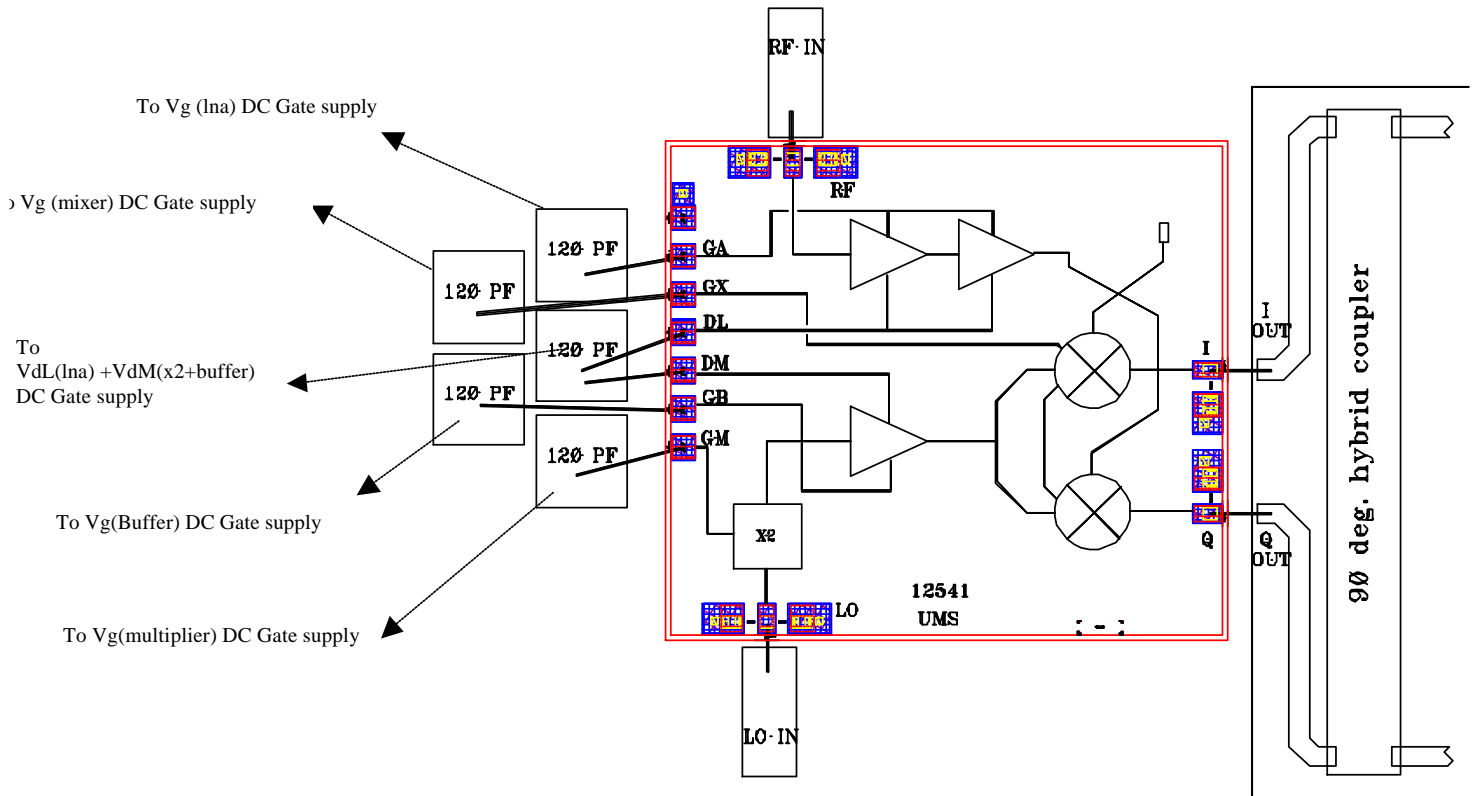
Conversion gain & Image suppression with a 90° IQ combiner



Gain compression versus RF input power



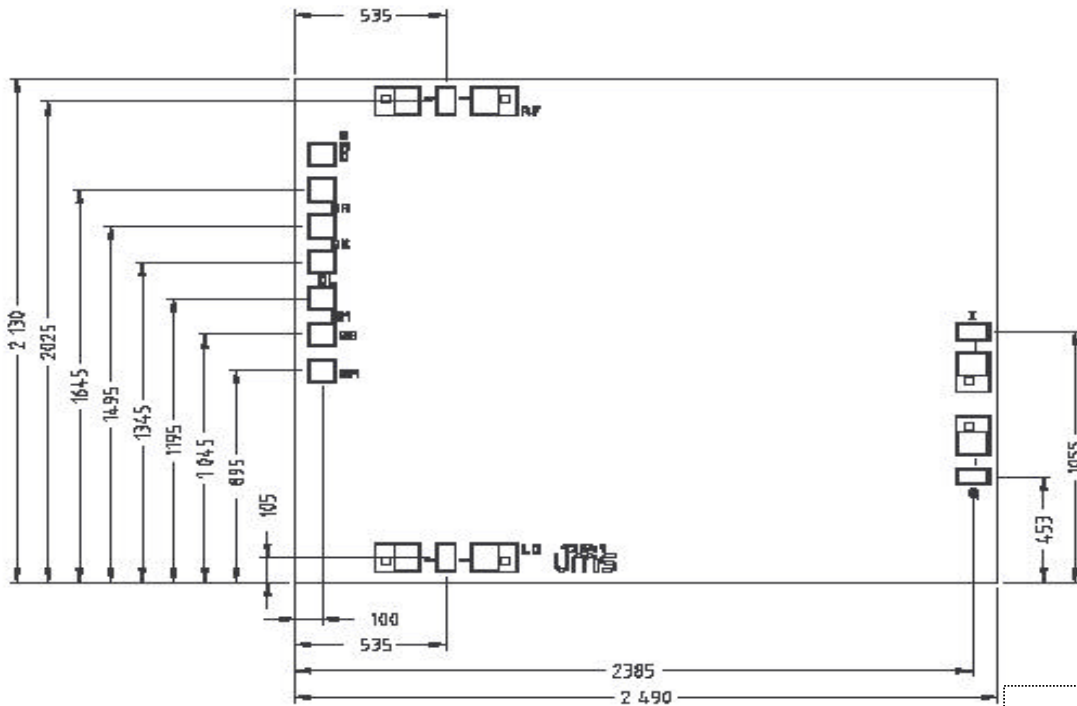
Chip Assembly and Mechanical Data



Note : Supply feed should be capacitively bypassed. 25µm diameter gold wire is recommended

Bonding pad positions

Chip thickness : 100µm



Unit : µm
Tol : +/- 35µm

Ordering Information

Chip form : CHR2391-99F/00

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