

X-band HBT High Power Amplifier

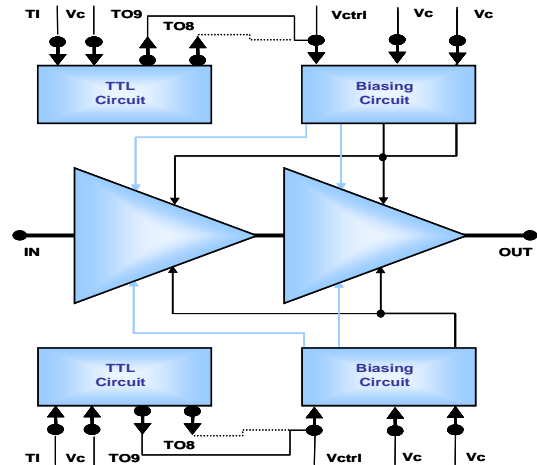
GaAs Monolithic Microwave IC

Preliminary

Description

The CHA8100 chip is a monolithic two-stage high power amplifier designed for X band applications. The HPA provides typically 11W output power, 40% power added efficiency and a high robustness on mismatched output. Moreover it includes:

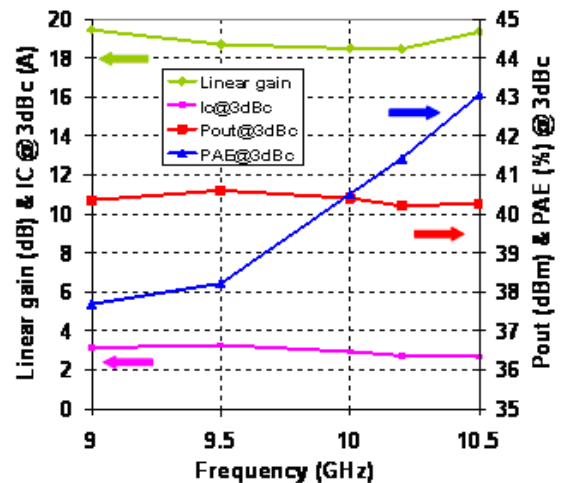
- an analogue biasing circuit that makes it less sensitive to spread and chip environment.
- an integrated TTL interface that enables to switch the HPA with a current consumption lower than 1mA



The circuit is 100% DC and RF tested on wafer to ensure performance compliance. This device is manufactured using a GaInP HBT process, including, via holes through the substrate and air bridges.

Main Features

- 11W output power in pulse mode
- High gain: > 18dB @ 10GHz
- High PAE: 40% @ 10GHz
- Two biasing modes:
 - Digital control thanks to TTL interface
 - Analog control thanks to biasing circuit
- Chip size: 4.9 x 3.68 x 0.1mm³



Main Characteristics

Vc=9V, Ic (Quiescent) = 2.1A, Pulse width=100μs, Duty cycle = 20%

Symbol	Parameter	Min	Typ	Max	Unit
Top	Operating temperature range (1)	-40		+80	°C
F_op	Operating frequency range	9		10.5	GHz
P_sat	Saturated output power @ 25°C		12.5		W
P_3dBc	Output power @ 3dBc @ 25°C		11		W
G_lin	Linear gain @ 25°C		18		dB

ESD Protections: Electrostatic discharge sensitive device. Observe handling precautions!

(1) The reference is the back-side of the chip.

Preliminary

Electrical Characteristics

Tamb = 25°C, Vc=9V, Ic (Quiescent) = 2.1A, Pulse width=100µs, Duty cycle = 20%

Symbol	Parameter	Min	Typ	Max	Unit
F_op	Operating frequency	9		10.5	GHz
G_lin	Linear gain		18		dB
G_lin_T	Linear gain variation versus temperature		-0.025		dB/°C
RL_in	Input Return Loss		-9		dB
RL_out	Output Return Loss		-15		dB
P_sat	Saturated output power		41		dBm
P_sat_T	Saturated output power variation versus temperature		-0.01		dB/°C
P_3dBc	Output power @ 3dBc (3)		40.5		dBm
PAE_3dBc	Power Added Efficiency @ 3dBc		40		%
Vc	Power supply voltage (3)	8		9	V
Ic	Power supply quiescent current (1)		2.1		A
TI	TTL input voltage	0		5	V
I_TI	TTL input current		0.7		mA
Vctrl	Collector current control voltage		5		V
Ictrl	Control supply current		22		mA
Zctr	Vctrl input port impedance (2)		350		Ohm
Top	Operating temperature range	-40		+80	°C

(1) Parameter tunable by Vctrl when control biasing circuit used.

(2) This value corresponds to the 4 ports in parallel

(3) 0.5V variation on Vc leads to around 0.4dB variation of the output power (impact on robustness see Maximum ratings)

Absolute Maximum Ratings (1)

Tamb = 25°C

Symbol	Parameter	Values	Unit
Cmp	Compression level (2 & 3)	8	dB
Vc	Power supply voltage (4)	10	V
Ic	Power supply quiescent current	3	A
Ic_sat	Power supply current in saturation	4	A
Vctrl	Collector current control voltage	6.5	V
Tj	Maximum junction temperature (5)	175	°C
Tstg	Storage temperature range	-55 to +125	°C

(1) Operation of this device above any one of these parameters may cause permanent damage.

(2) For higher compression the level limit can be raised by decreasing the voltage Vc using the rate 0.5 V / dBc

(3) Vc=9V, Temperature=-40°C, Output VSWR=2:1

(4) Without RF input power

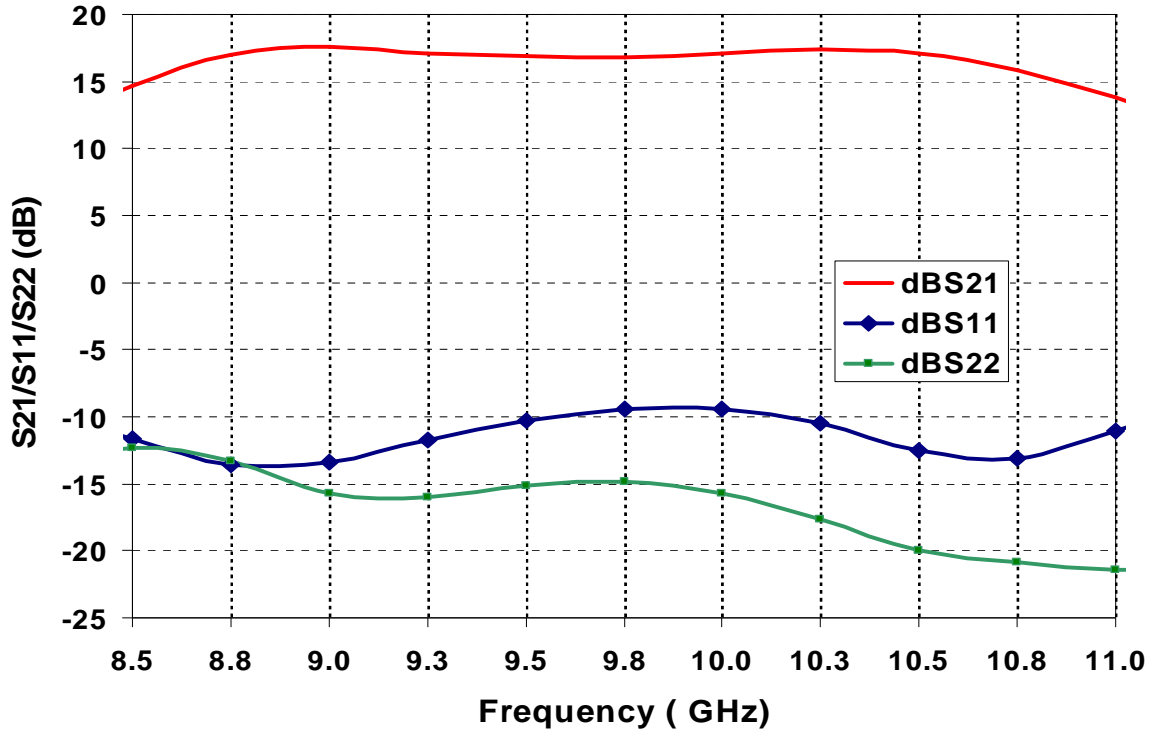
(5) Equivalent Thermal resistance to Backside: 6°C/W

Typical measured characteristics

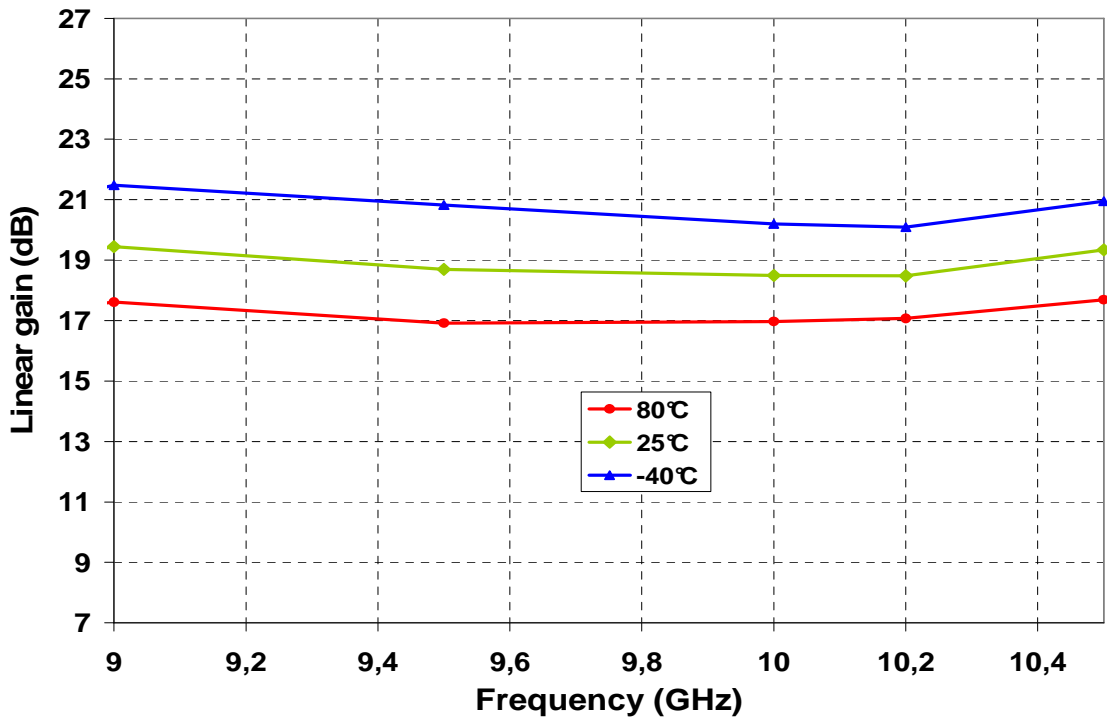
Preliminary

Measurements on Jig:

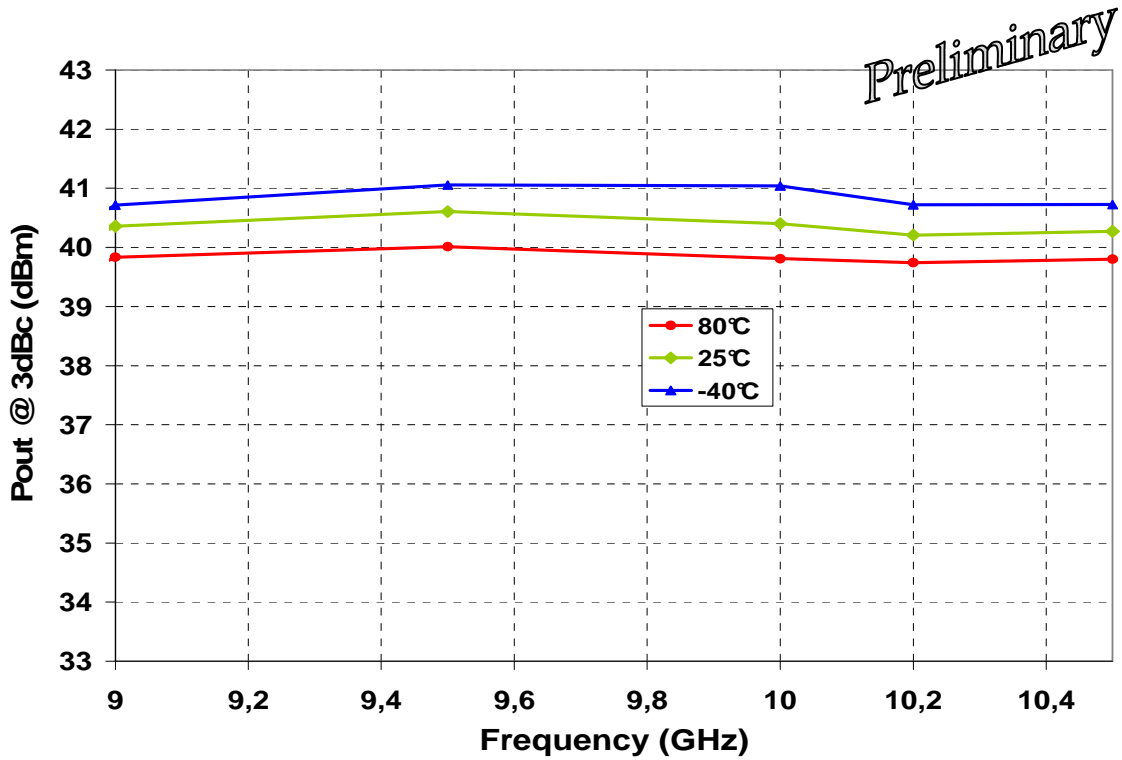
V_c = 9V, V_{TTL}=5V, I_c (Quiescent) = 2.1A, Pulse width=100μs, Duty cycle = 20%



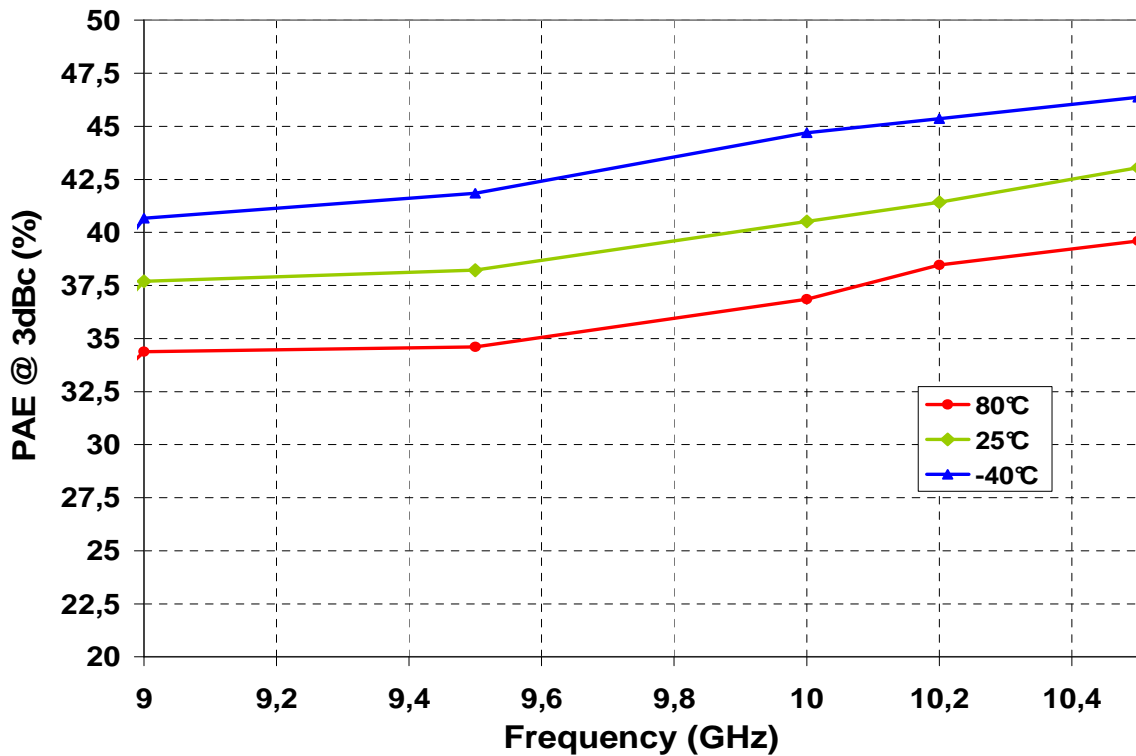
Gain/Input & Output Return losses (dB). Temperature: +20°C



Linear Gain versus frequency and temperature

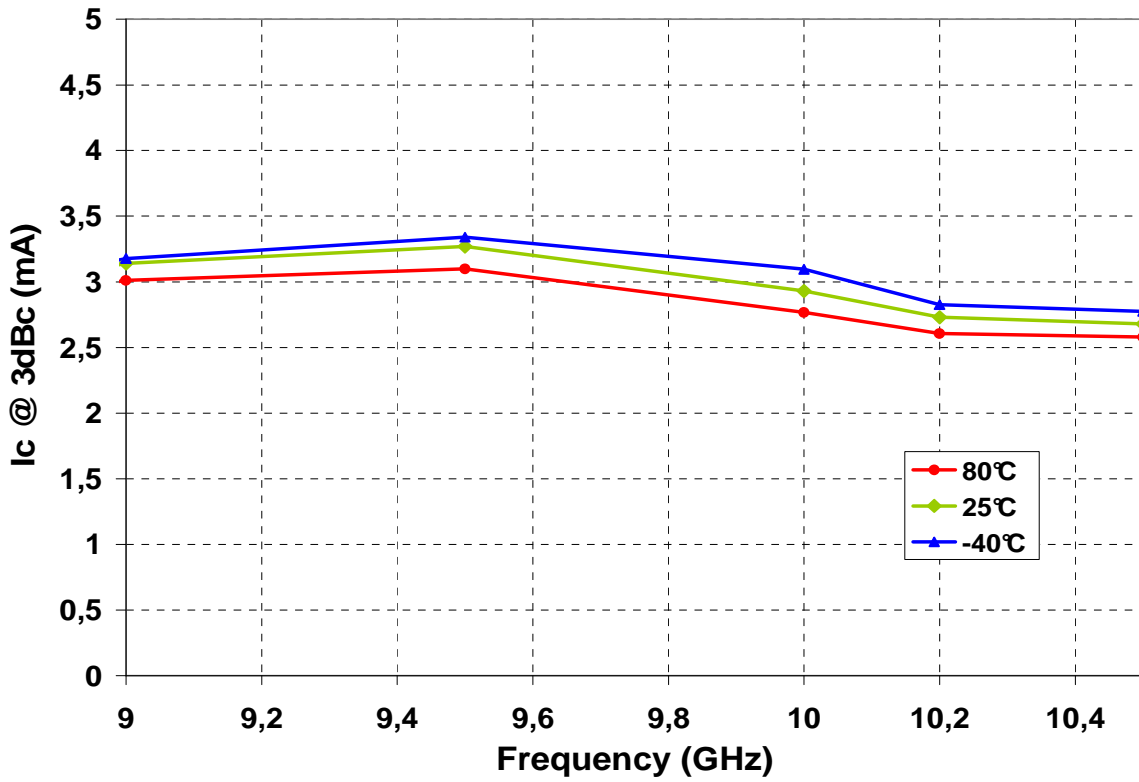


Output Power @ 3dBc versus frequency and temperature

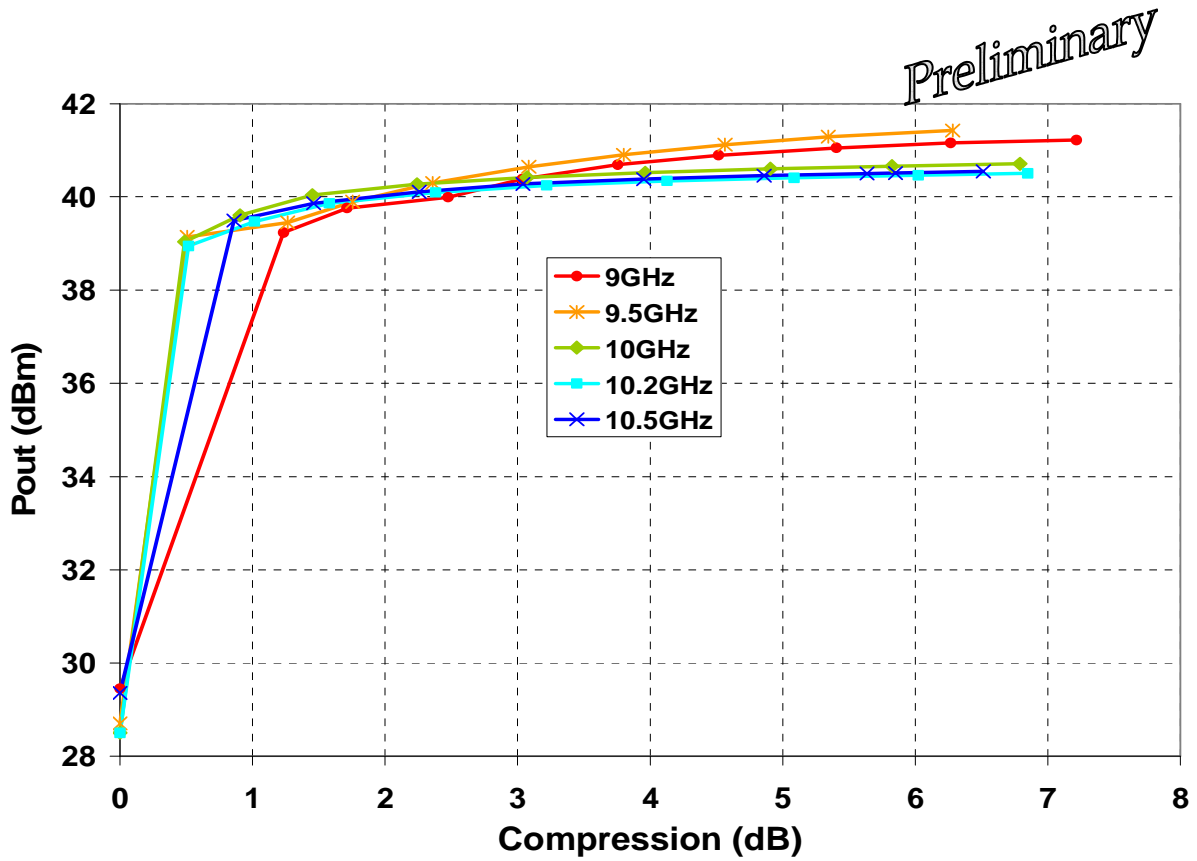


PAE @ 3dBc versus frequency and temperature

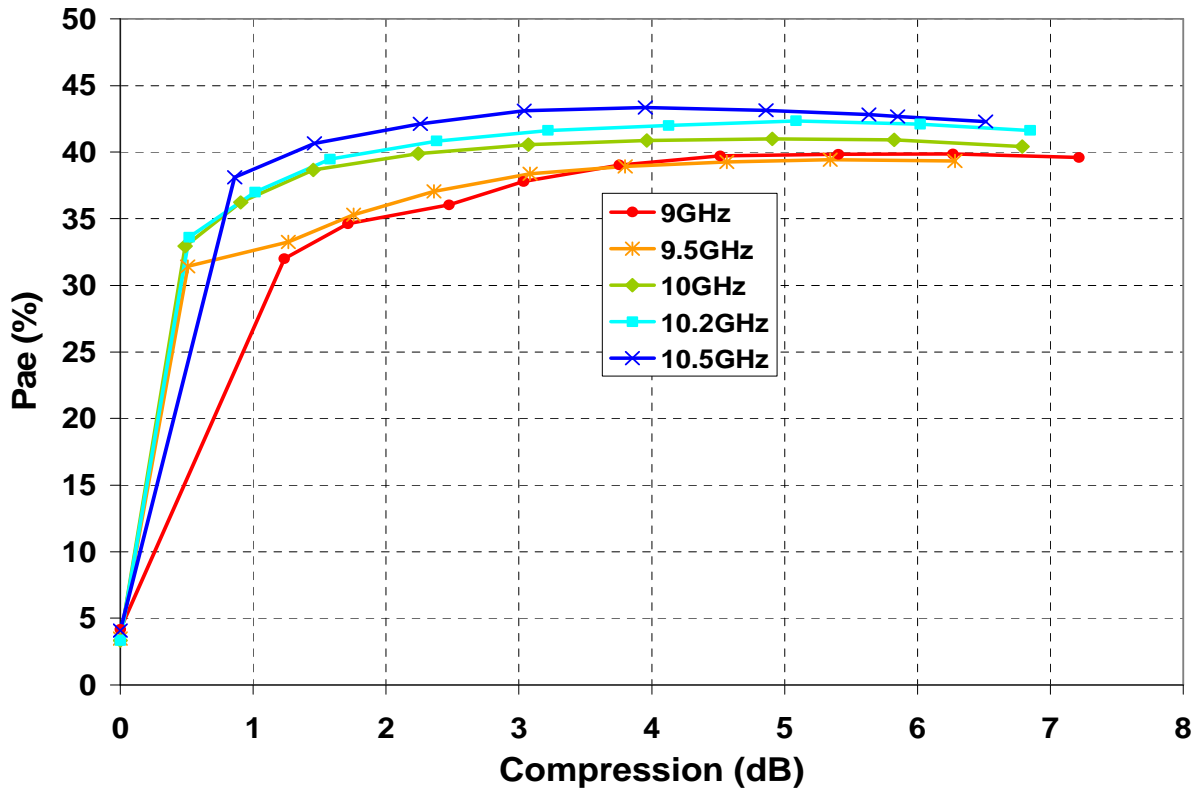
Preliminary



Ic @ 3dBc versus frequency and temperature

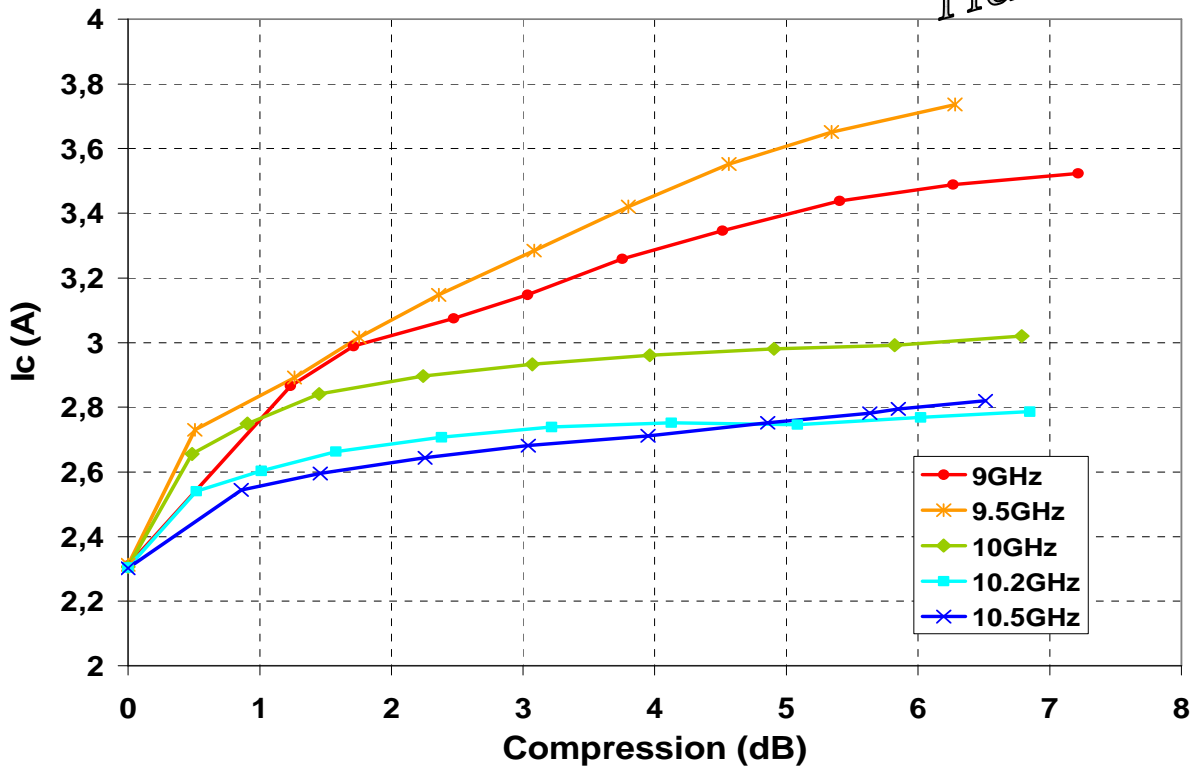


Output Power @ 25°C versus compression and frequency

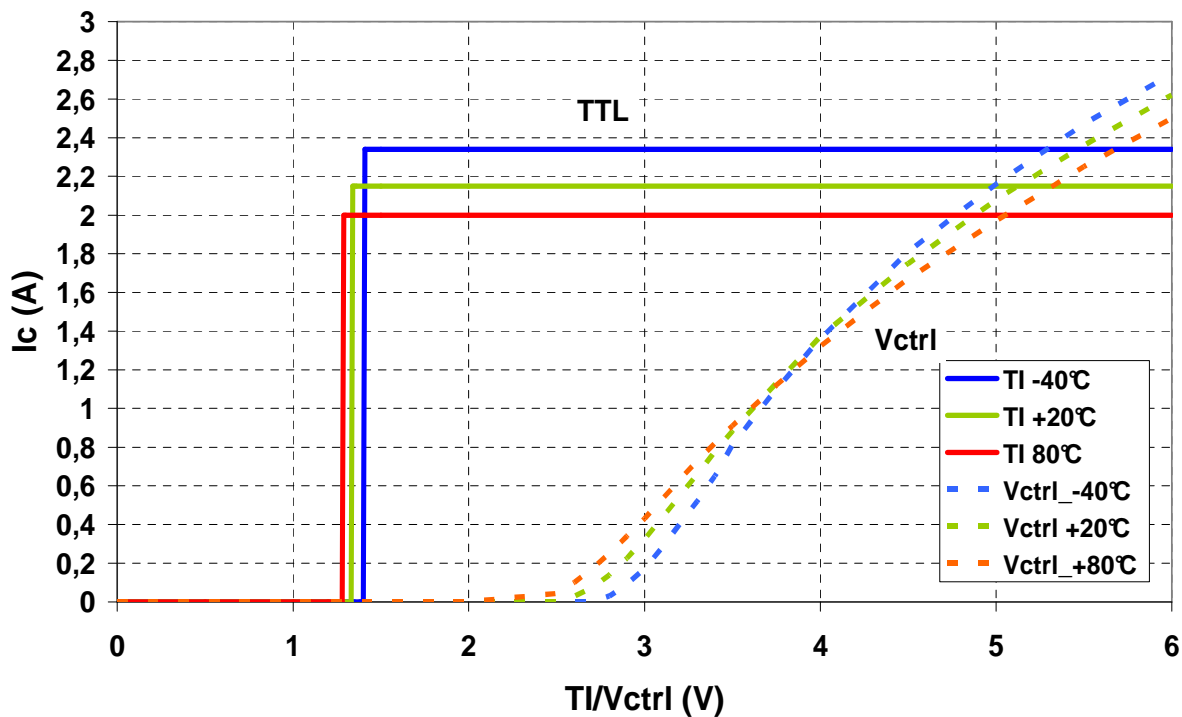


PAE @ 25°C versus compression and frequency

Preliminary

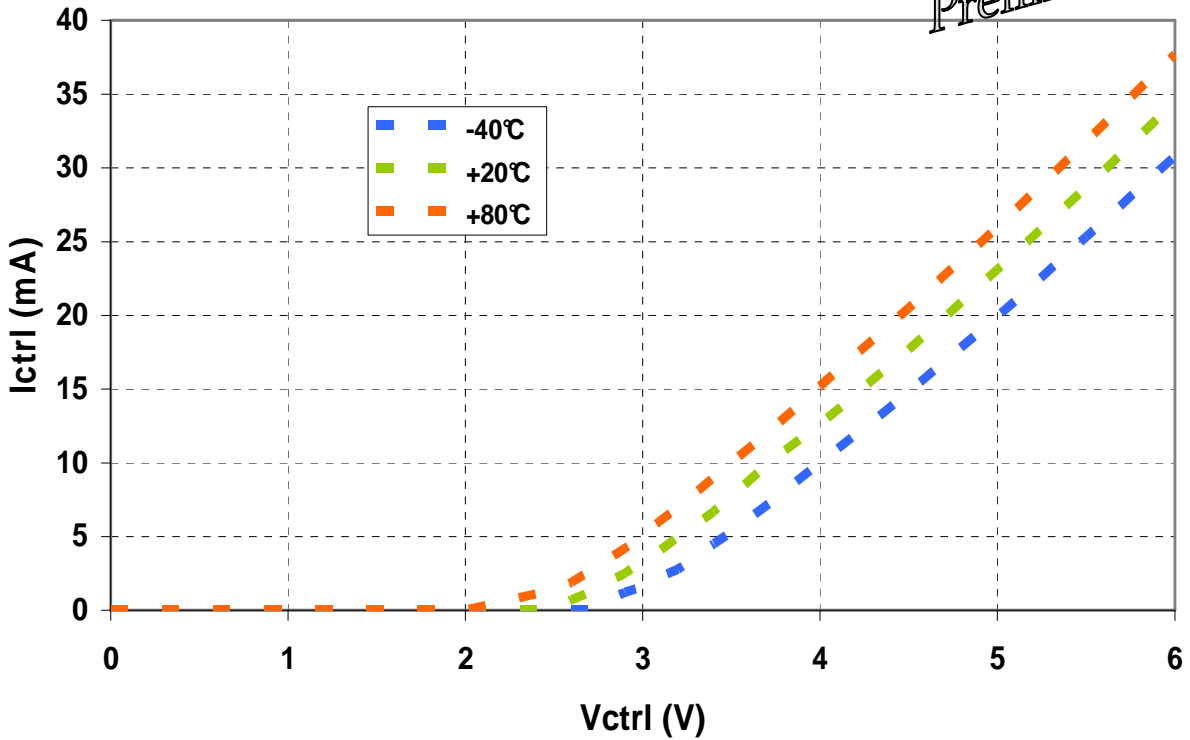


Collector current @ 25°C versus compression and frequency



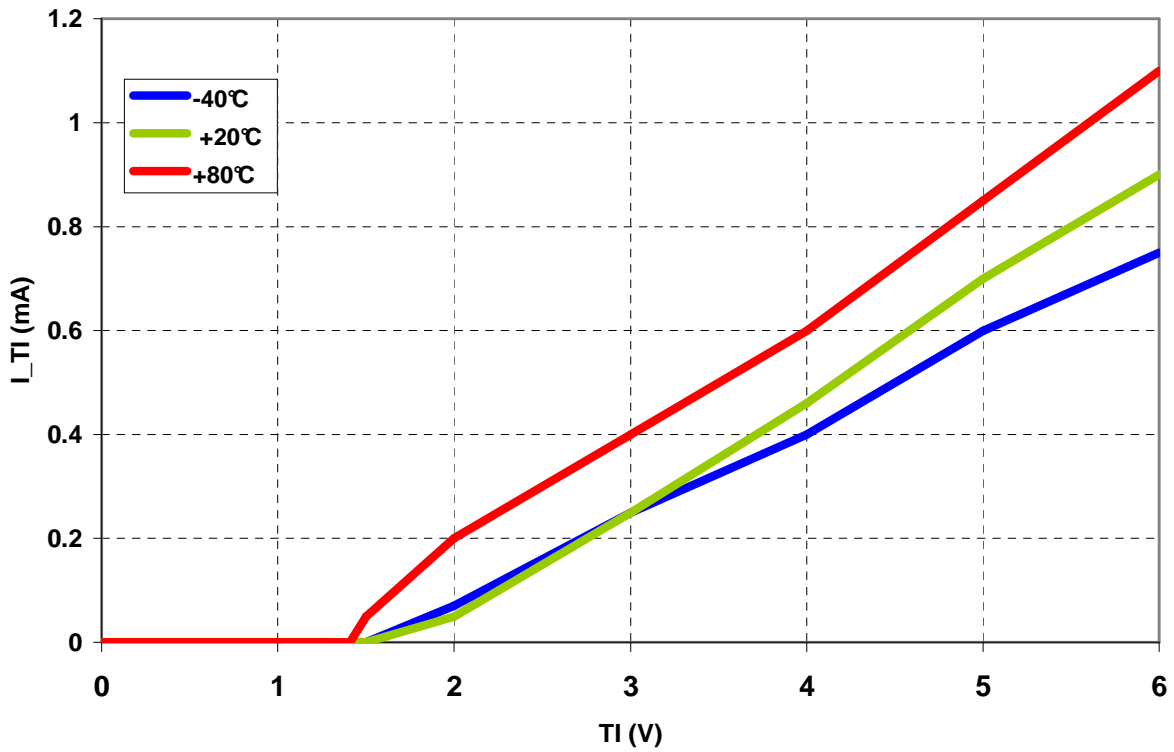
Collector quiescent current versus TI & Vctrl and temperature

Preliminary



Control current versus control voltage & temperature

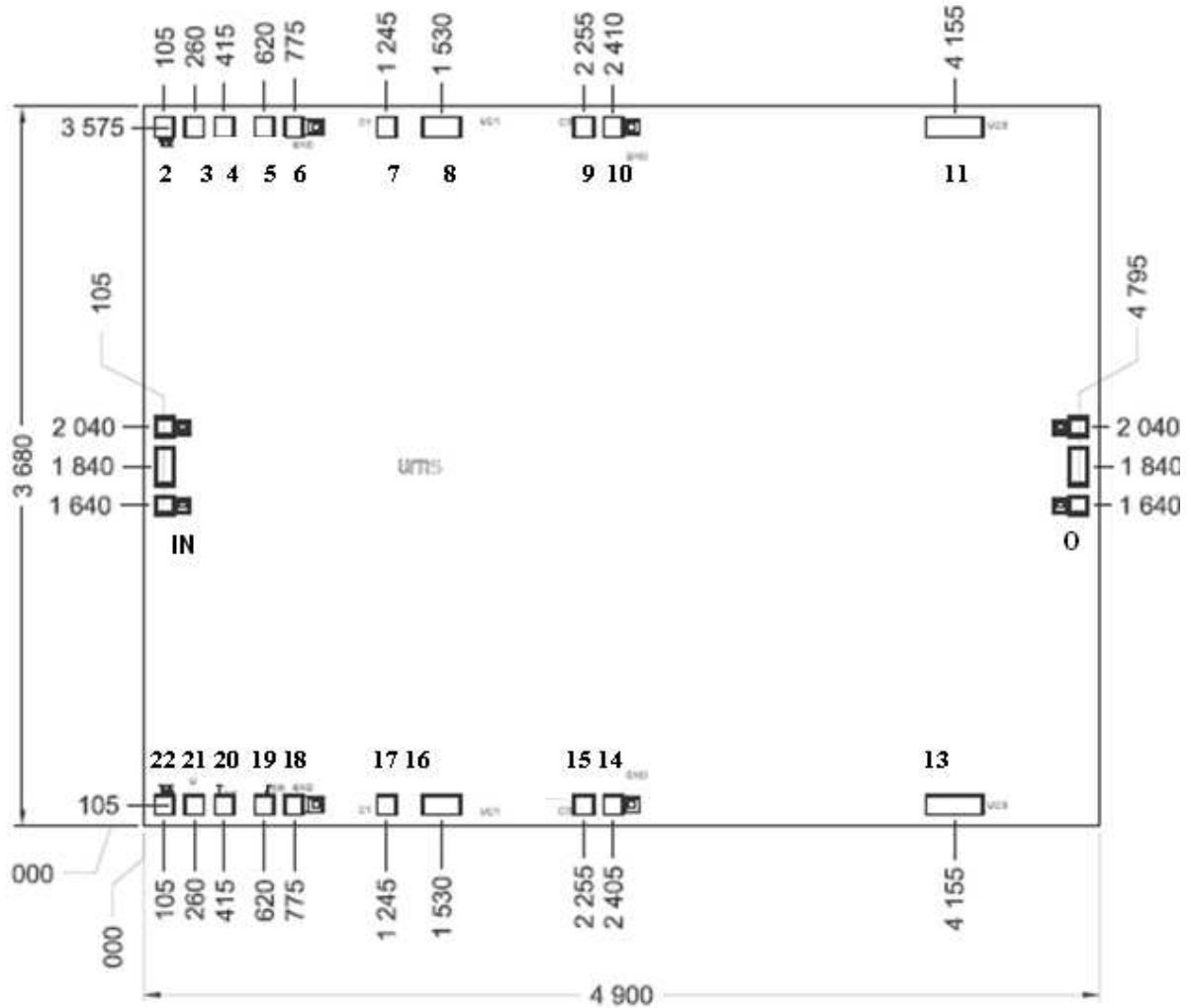
$I_{TI}(V)$



TTL input current versus TTL voltage and temperature

Preliminary

Chip Mechanical Data and Pin references



Units: μm

Chip width and length are given with a tolerance of $\pm 35\mu\text{m}$

Chip thickness = $100\mu\text{m} \pm 10\mu\text{m}$

RF pads (1, 12) = $96 \times 196\mu\text{m}^2$

DC pads (2, 3, 4, 5, 6, 7, 9, 10, 14, 15, 17, 18, 19, 20, 21, 22) = $96 \times 96\mu\text{m}^2$

DC pads (8, 16) = $192 \times 96\mu\text{m}^2$

DC pads (11, 13) = $288 \times 96\mu\text{m}^2$

Pin number	Pin name	Description
1	IN	Input RF
7, 9, 15, 17	C1, C2	Collector current control voltage
2, 22	TI	TTL input
4, 20	TO9	TTL output when $V_{cx}=9V$
5, 19	TO8	TTL output $V_{cx}=8V$
6, 10, 14, 18	GND	Ground (NC)
3, 8, 11, 13, 16, 21	V, Vc1, Vc2	Power supply voltage
12	OUT	Output RF

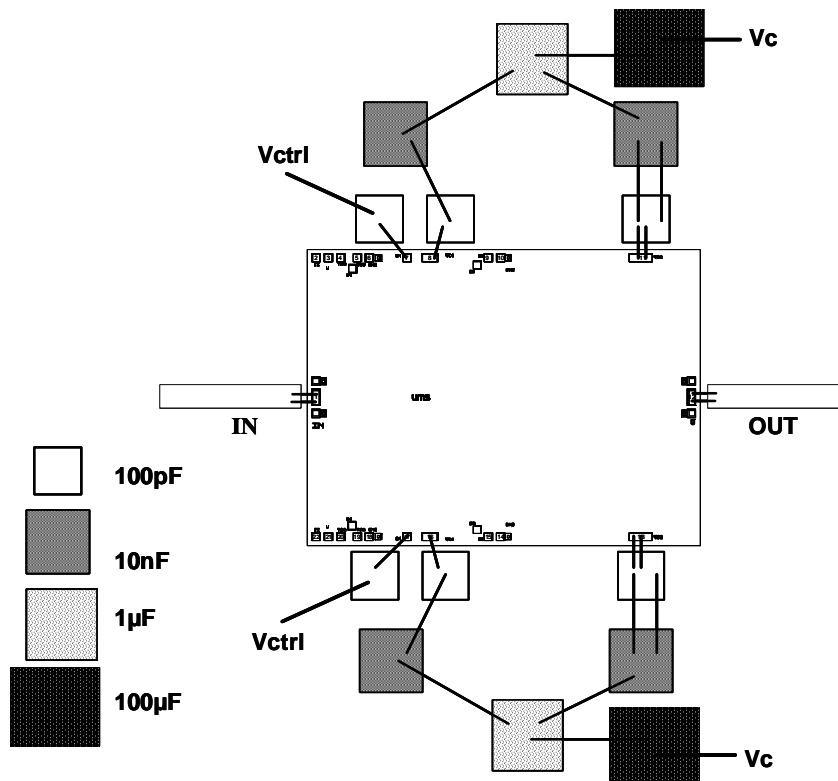
Preliminary

Bonding recommendations

For thermal and electrical considerations, the chip should be brazed on a metal base plate. The RF, DC and modulation port inter-connections should be done according to the following table:

Port	Connection
IN (1)	Inductance (L_{bonding}) = 0.3nH 400 μm length with wire diameter of 25 μm x2
OUT (12)	Inductance (L_{bonding}) = 0.3nH 400 μm length with wire diameter of 25 μm x2
DC pads to 1 st decoupling level for double bonding	Inductance (L_{bonding}) = 0.7nH Two 1.2mm length wires with a diameter of 25 μm
DC pads to 1 st decoupling level for single bonding	Inductance (L_{bonding}) = 1nH One 1.2mm length wires with a diameter of 25 μm
1 st decoupling level to 2 nd decoupling level for double bonding	Inductance (L_{bonding}) = 0.7nH Two 1.2mm length wires with a diameter of 25 μm
1 st decoupling level to 2 nd decoupling level for single bonding	Inductance (L_{bonding}) = 1nH One 1.2mm length wires with a diameter of 25 μm

Assembly recommendations in test fixture (using analogue biasing circuits)

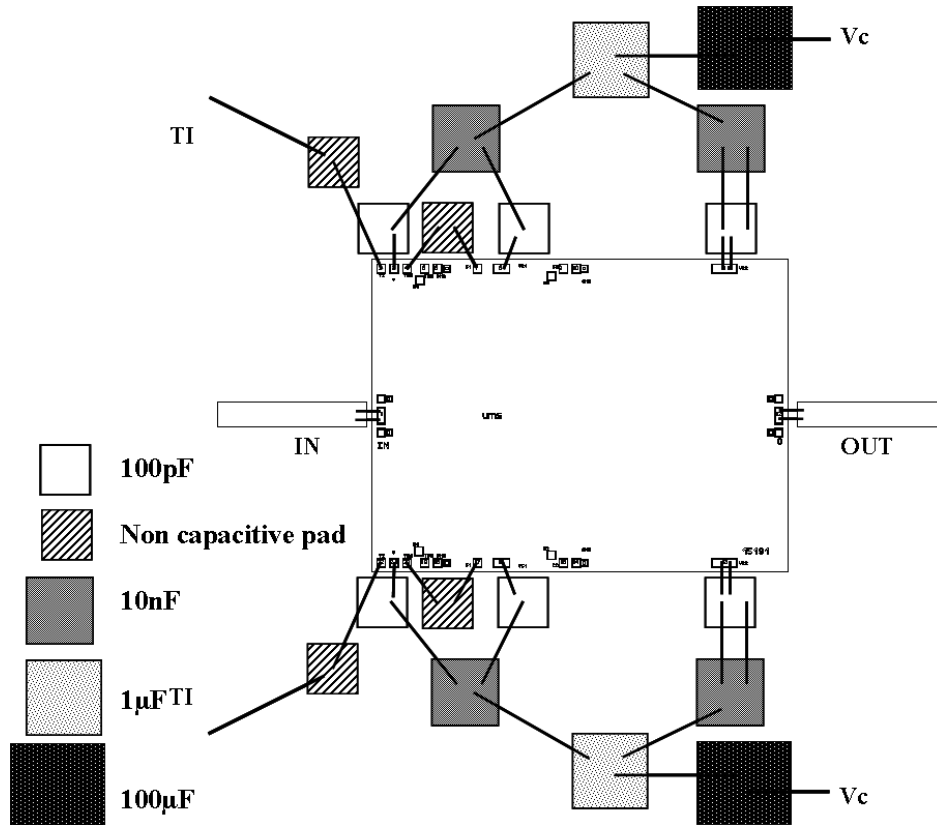


Note: Supply feed should be capacitively by-passed. 25 μm diameter gold wire is to be preferred.



Preliminary

**Assembly recommendations in test fixture
(using TTL circuits)**



* Performances obtained with the same accesses connected to the same supply
Note: Supply feed should be capacitively by-passed. 25µm diameter gold wire is to be preferred.

Biasing possibilities

TTL / Vcontrol	V _{C1} , V _{C2} , V	Connections
Biasing via TTL interface	9V	T09 connected to C1 and C2 C2 & T08 not connected
Biasing via TTL interface	8V	T08 connected to C1 and C2 C2 & T09 not connected
Biasing via analogue control device	9V or 8V	C2, V, Ti, T08, T09 not connected

Preliminary

Ordering Information

Chip form : CHA8100-99F/00

Information furnished is believed to be accurate and reliable. However **United Monolithic Semiconductors S.A.S.** assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of **United Monolithic Semiconductors S.A.S.** Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. **United Monolithic Semiconductors S.A.S.** products are not authorised for use as critical components in life support devices or systems without express written approval from **United Monolithic Semiconductors S.A.S.**