

# X Band High Power Amplifier

## GaAs Monolithic Microwave IC

Preliminary

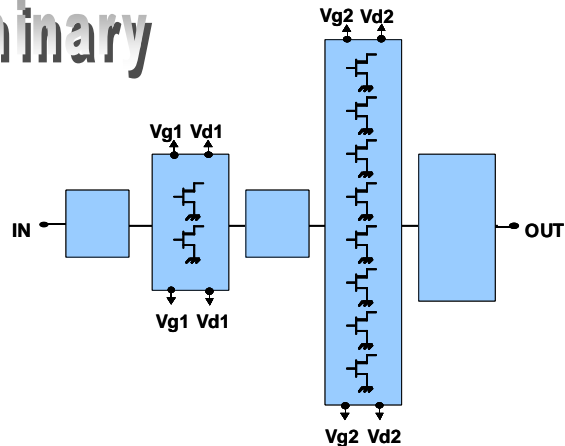
### Description

The CHA7114 is a monolithic two-stage GaAs high power amplifier designed for X band applications.

This device is manufactured using a UMS 0.25  $\mu\text{m}$  power pHEMT process, including, via holes through the substrate and air bridges.

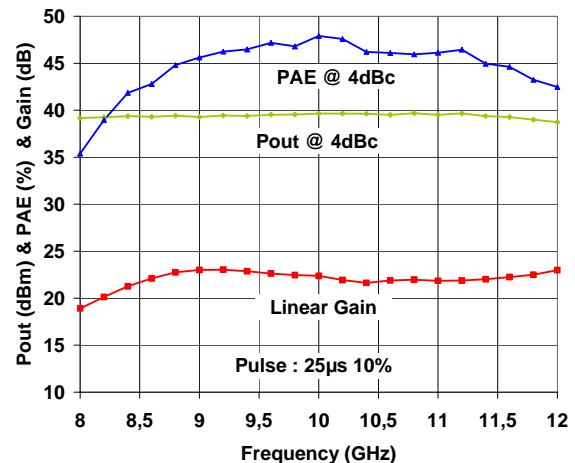
To simplify the assembly process:

- The backside of the chip is both RF and DC grounded
- Bond pads and back side are gold plated for compatibility with eutectic die attach method and thermo-compression bonding process.



### Main Features

- 0.25 $\mu\text{m}$  Power pHEMT Technology
- 8.5–11.5GHz Frequency Range
- 8W Output Power @ 4dBc
- High PAE: > 40% @ 4dBc
- 20dB nominal Gain
- Quiescent Bias point:  $V_d = 8\text{V}$ ,  $I_d = 2\text{A}$
- Chip size: 4.41mm x 3.31mm x 0.07mm



### Main Characteristics

$T_{amb} = +25^\circ\text{C}$  ( $T_{amb}$  is the back-side of the chip)

$V_d = 8\text{V}$ ,  $I_d$  (Quiescent) = 2A, Pulse width = 25 $\mu\text{s}$ , Duty cycle = 10%

Symbol	Parameter	Min	Typ	Max	Unit
Top	Operating temperature range	-40		+80	$^\circ\text{C}$
Fop	Operating frequency range	8.5		11.5	GHz
P_4dBc	Output power @ 4dBc @ 25 $^\circ\text{C}$		8		W
G	Small signal gain @ 25 $^\circ\text{C}$		20		dB

ESD Protections: Electrostatic discharge sensitive device. Observe handling precautions!

## Electrical Characteristics

Tamb = 25°C, Vd = 8V, Id (Quiescent) = 2A, Pulse width = 25µs, Duty cycle=10%

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency	8.5		11.5	GHz
G	Small signal gain	17.5	20	23	dB
G_T	Small signal gain variation versus temperature		-0.033		dB/°C
RLin	Input Return Loss	8	10		dB
RLout	Output Return Loss	6	8		dB
Psat	Saturated output power		39.8		dBm
Psat_T	Saturated output power variation versus temperature		-0.008		dB/°C
P_4dBc	Output power @ 4dBc (2)	38	39		dBm
PAE_4dBc	Power Added Efficiency @ 4dBc	36	42		%
Id	Supply drain current		2.3	2.6	A
Vd1, Vd2	Drain supply voltage (2)		8.0	8.5	V
Id_q	Supply quiescent drain current (1)		2.0		A
Vg1, Vg2	Gate Power supply voltage		-4.0		V
Top	Operating temperature range	-40		+80	°C

(1) Parameter to be adjusted by tuning of Vg

(2) 0.5V variation on Vd leads to around 0.4dB variation of the output power (impact on robustness see Maximum ratings)

## Absolute Maximum Ratings (1)

Tamb = 25°C

Symbol	Parameter	Values	Unit
Cmp	Compression level (2)	6	dB
Vd	Drain Power supply voltage (3)	10	V
Id	Drain Power supply quiescent current	2.5	A
Id_sat	Drain Power supply current in saturation	3	A
Vg	Gate Power supply voltage	-8	V
Tj	Maximum junction temperature (4)	175	°C
Tstg	Storage temperature range	-55 to +125	°C

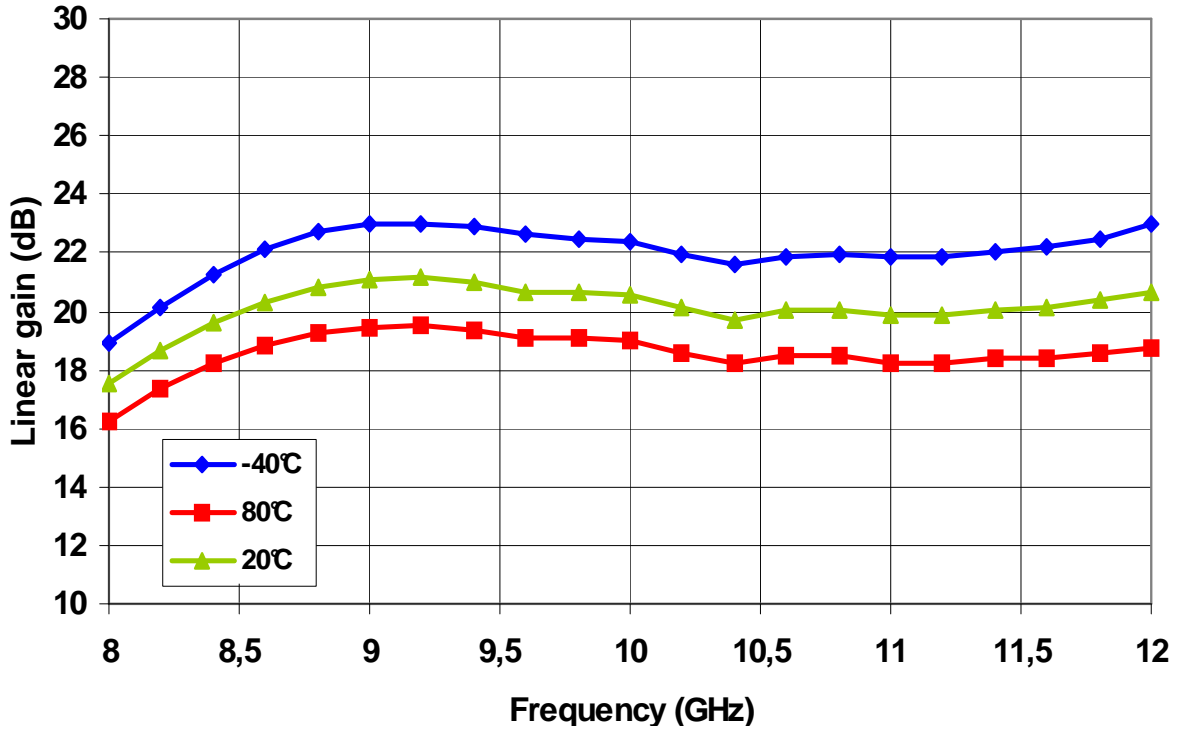
- (1) Operation of this device above anyone of these parameters may cause permanent damage.
- (2) For higher compression the level limit can be increased by decreasing the voltage Vd using the rate 0.5 V / dBc
- (3) Without RF input power
- (4) Equivalent Thermal Resistance to Backside: 5.6°C/W for backside temp. of 80°C.  
*[ Junction Temperature comes from:  $T_j = T_{backside} + ETRB \times (\text{Dissipated Power})$   
 Where **ETRB** stands for **E**quivalent **T**hermal **R**esistance to **B**ackside. ]*

Typical measured characteristics

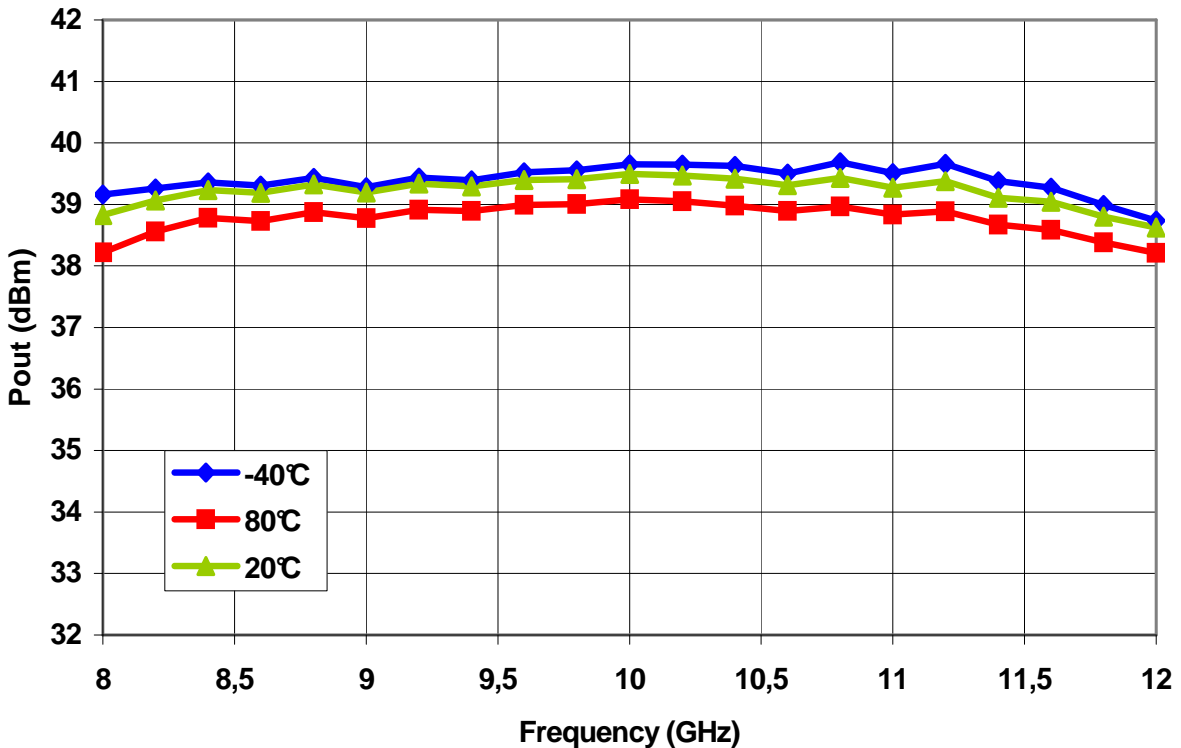
Preliminary

Measurements on Jig:

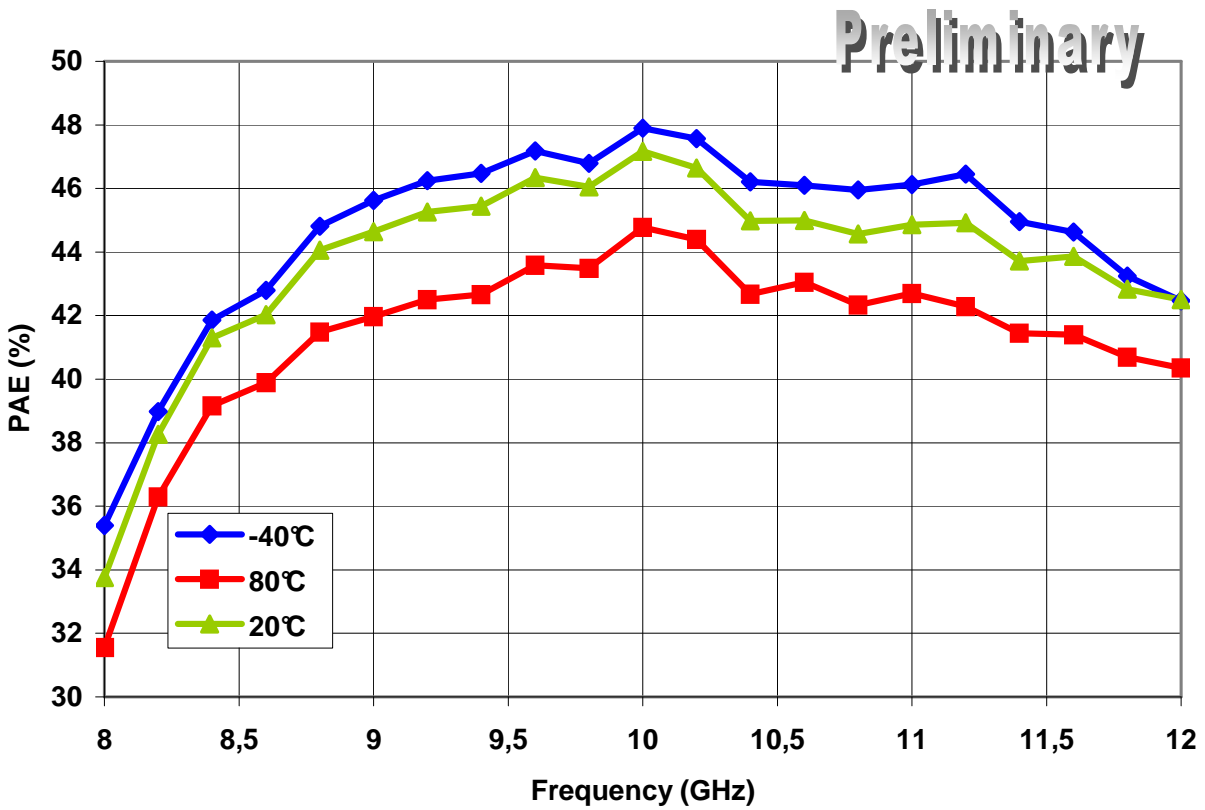
Vd = 8V, Vg = -4.0V, Id (Quiescent) = 2.2A, Pulse width = 25µs, Duty cycle = 10%



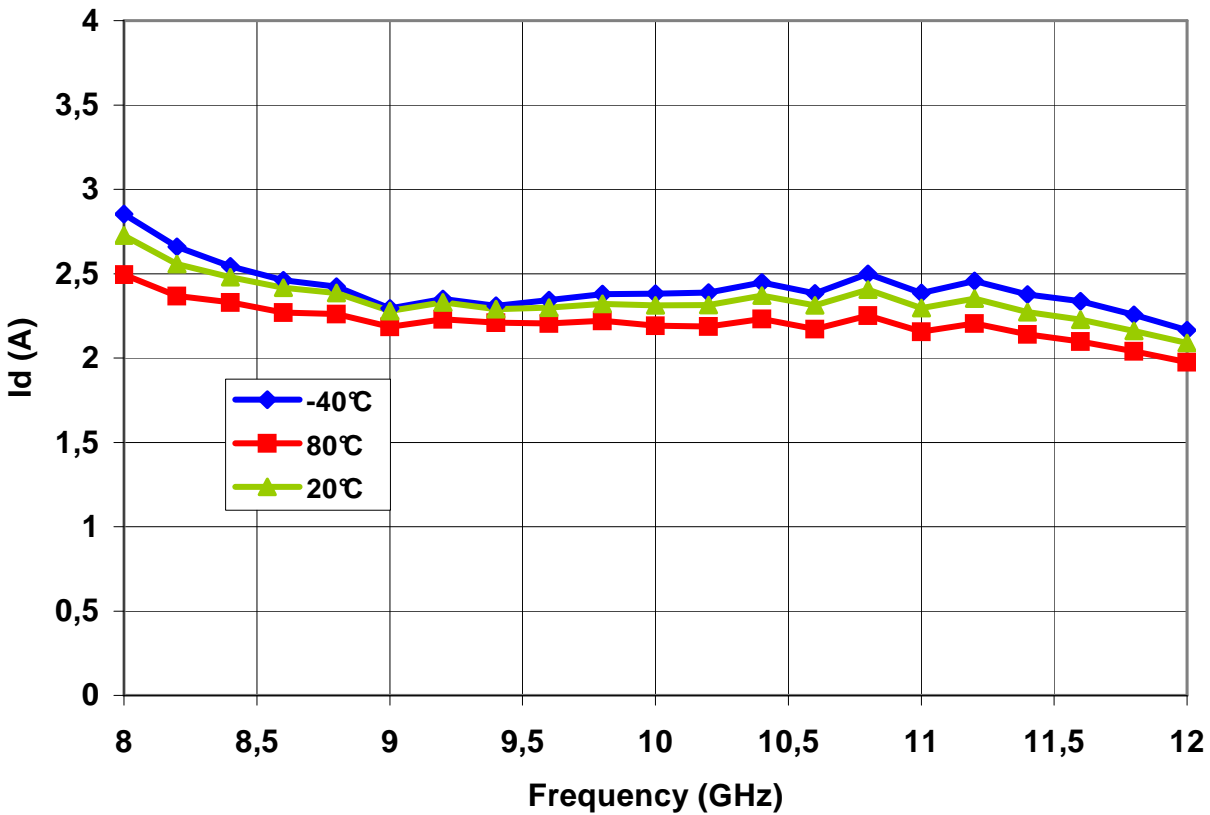
Linear gain versus frequency and temperature



Output Power @ 4dBc versus frequency and temperature

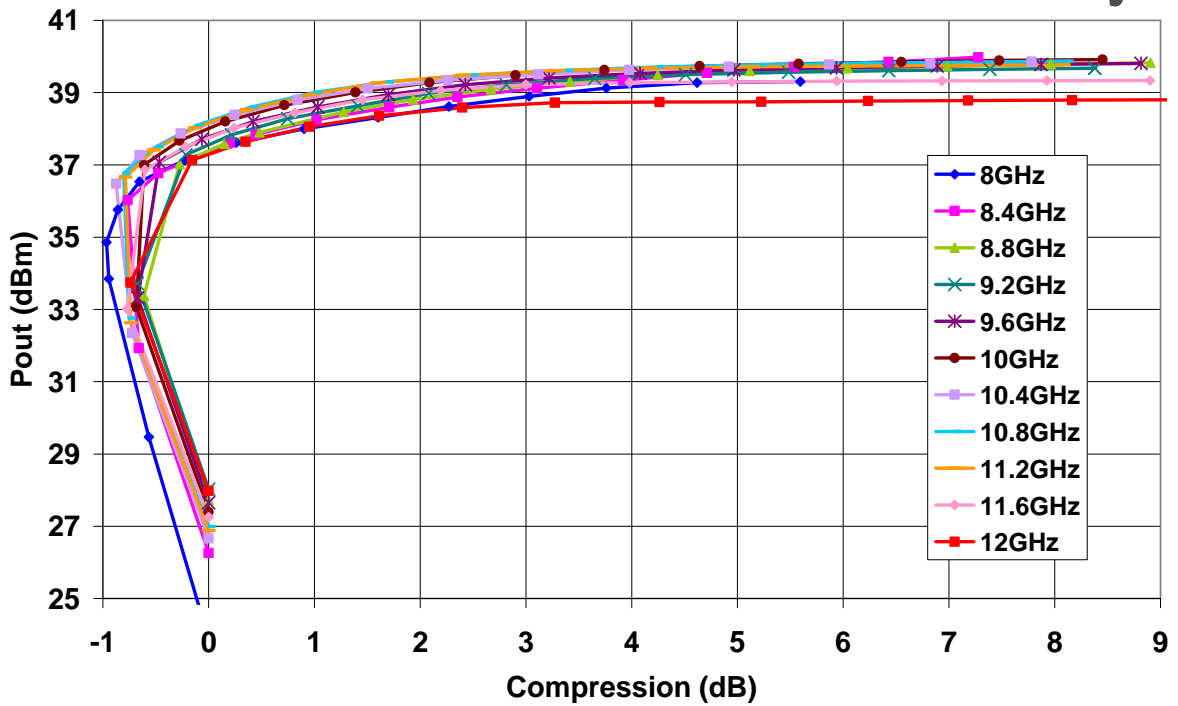


PAE @ 4dBc versus frequency and temperature

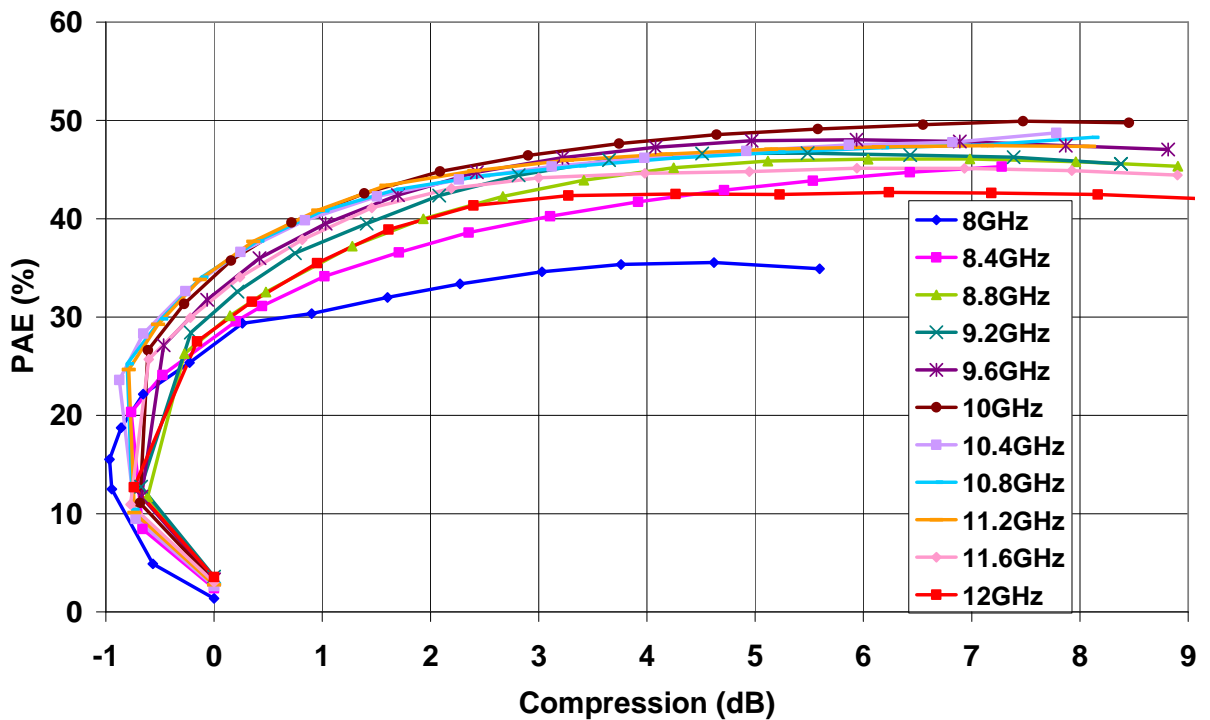


Id @ 4dBc versus frequency and temperature

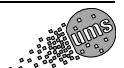
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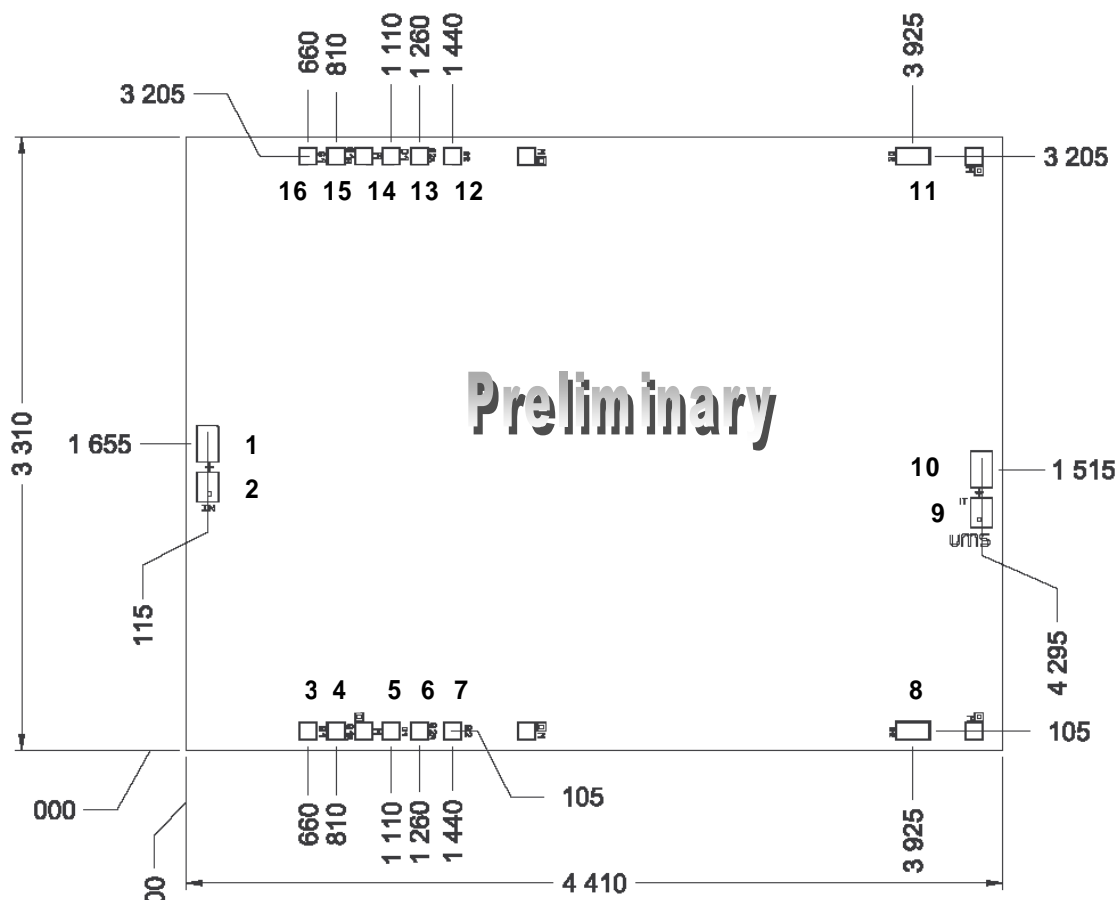


Output Power @ 25°C versus compression and frequency



PAE @ 25°C versus compression and frequency





## Chip Mechanical Data and Pin references

Chip width and length are given with a tolerance of +/- 35µm

Chip thickness = 70µm +/- 10µm

HF pads (1, 10) = 118µm x 196µm

DC pads (3, 4, 5, 6, 7, 12, 13, 14, 15, 16) = 96µm x 96µm

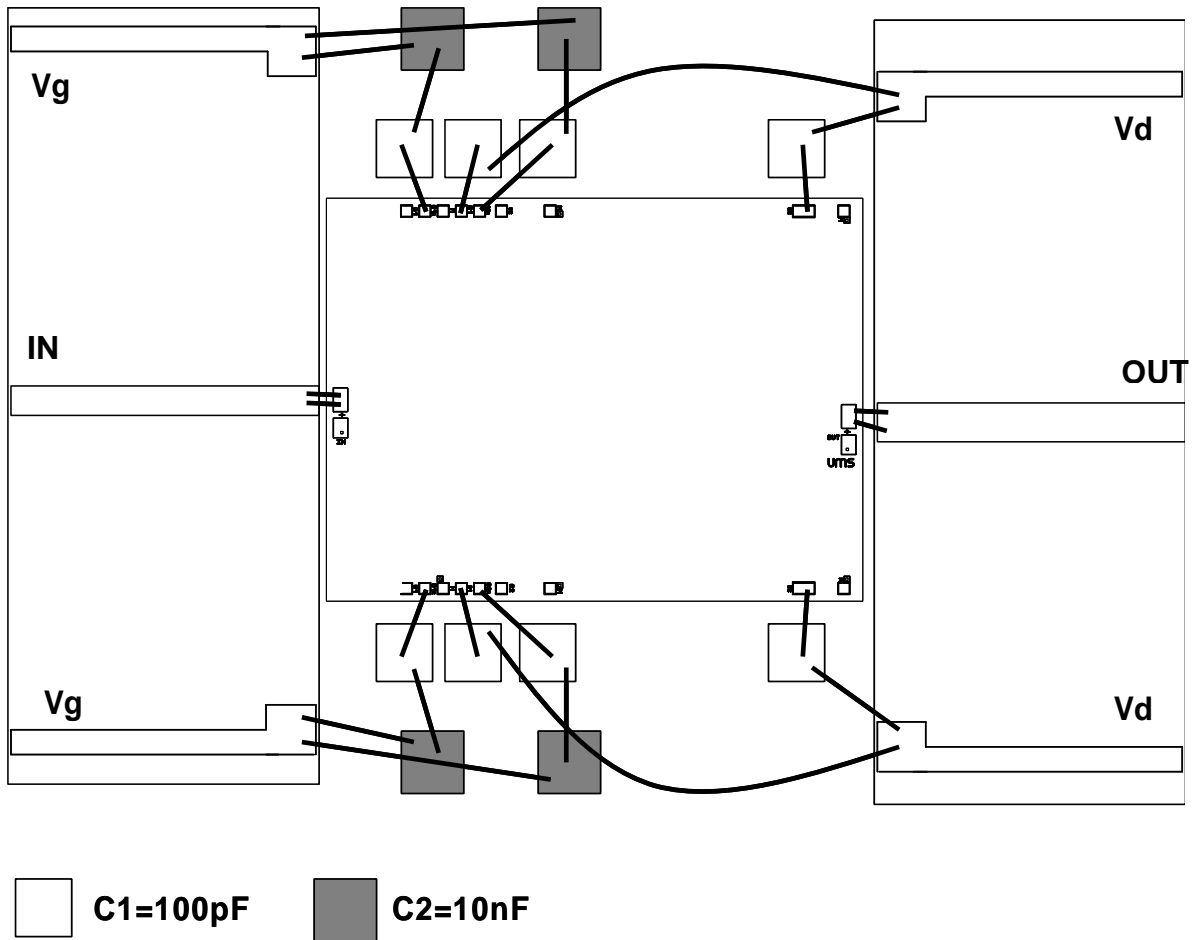
DC pads (8, 11) = 186µm x 96µm

Pin number	Pin name	Description
2, 9		Not Connected
3, 7, 12, 16	G1, G2	Not Connected
1	IN	Input RF port
4, 6, 13, 15	Vg1R, Vg2R	Vg: Negative supply voltage (through divided bridge Network)
5, 8, 11, 14	Vd1, Vd2	Vd: Positive supply voltage
10	OUT	Output RF port

Bonding recommendations

Port	Connection	External capacitor
IN	Inductance ( $L_{bonding}$ ) = 0.3nH 2 gold wires bondings (550 $\mu$ m max)	
OUT	Inductance ( $L_{bonding}$ ) = 0.3nH 2 gold wires bondings (550 $\mu$ m max)	
Vd1, Vd2	Inductance $\leq$ 1nH	C1 ~ 100pF
Vg1R, Vg2R	Inductance $\leq$ 1nH	C1 ~ 100pF C2 ~ 10nF

Assembly recommendations (drain voltage pulsed mode operation)



**Vg:** gate supply voltage  
**Vd:** drain supply voltage

## Ordering Information

Chip form:               CHA7114-99F/00

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