

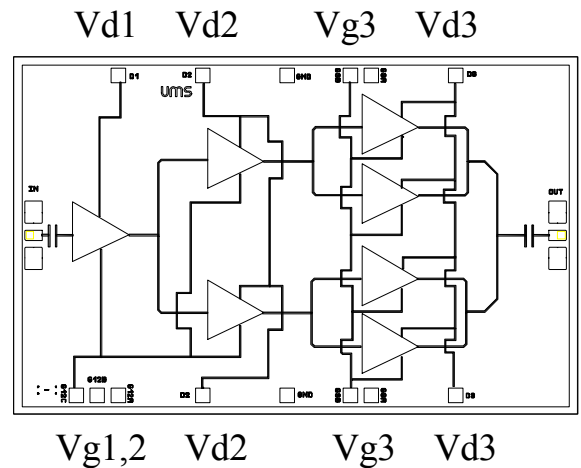
17-24GHz High Power Amplifier

GaAs Monolithic Microwave IC

Description

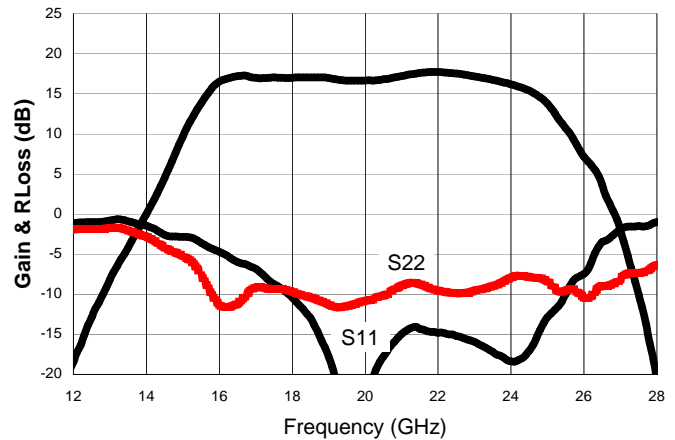
The CHA5293a is a high gain three-stage monolithic high power amplifier. It is designed for a wide range of applications, from military to commercial communication systems. The backside of the chip is both RF and DC grounds. This helps simplify the assembly process.

The circuit is manufactured with a PM-HEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography. It is available in chip form.



Main Features

- Wide band : 17-24GHz
- 31dBm output power @ 1dB comp. gain
- 18 dB ± 1dB gain
- DC power consumption, 800mA @ 6V
- Chip size : 4.01 x 2.52 x 0.05 mm



Typical on jig Measurements

Main Characteristics

Tamb. = 25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	17		24	GHz
G	Small signal gain	17	18		dB
P1dB	Output power at 1dB gain compression	30	31		dBm
Id	Bias current		800		mA

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

Electrical Characteristics

Tamb = +25°C, Vd = 6V Id #800mA

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range (1)	17		24	GHz
G	Small signal gain (1)	17	18		dB
ΔG	Small signal gain flatness (1)		±1		dB
Is	Reverse isolation		50		dB
P1dB	Pulsed output power at 1dB compression (1)	30	31		dBm
P03	Output power at 3dB gain compression (1)	32	33		dBm
IP3	3 rd order intercept point (2)		42		dBm
PAE	Power added efficiency at 1dB comp.		20		%
VSWRin	Input VSWR (2)			3:1	
VSWRout	Output VSWR (2)			3:1	
Tj	Junction temperature for 80°C backside		155		°C
Id	Bias current @ small signal		800	1000	mA

(1) These values are representative for pulsed on-wafer measurements that are made without bonding wires at the RF ports.

(2) Value representative for CW on jig measurement.

Absolute Maximum Ratings

Tamb. = 25°C (1)

Symbol	Parameter	Values	Unit
Vd	Maximum drain bias voltage with Pin max=12dBm	6.25	V
Id	Maximum linear drain bias current	1450	mA
Vg	Gate bias voltage	-2.5 to +0.4	V
Ig	Gate bias current	-5 to +5	mA
Vgd	Minimum negative gate drain voltage (Vg - Vd)	-8	V
Pin	Maximum input power overdrive (2)	15	dBm
Tch	Maximum channel temperature	175	°C
Ta	Operating temperature range	-40 to +80	°C
Tstg	Storage temperature range	-55 to +125	°C

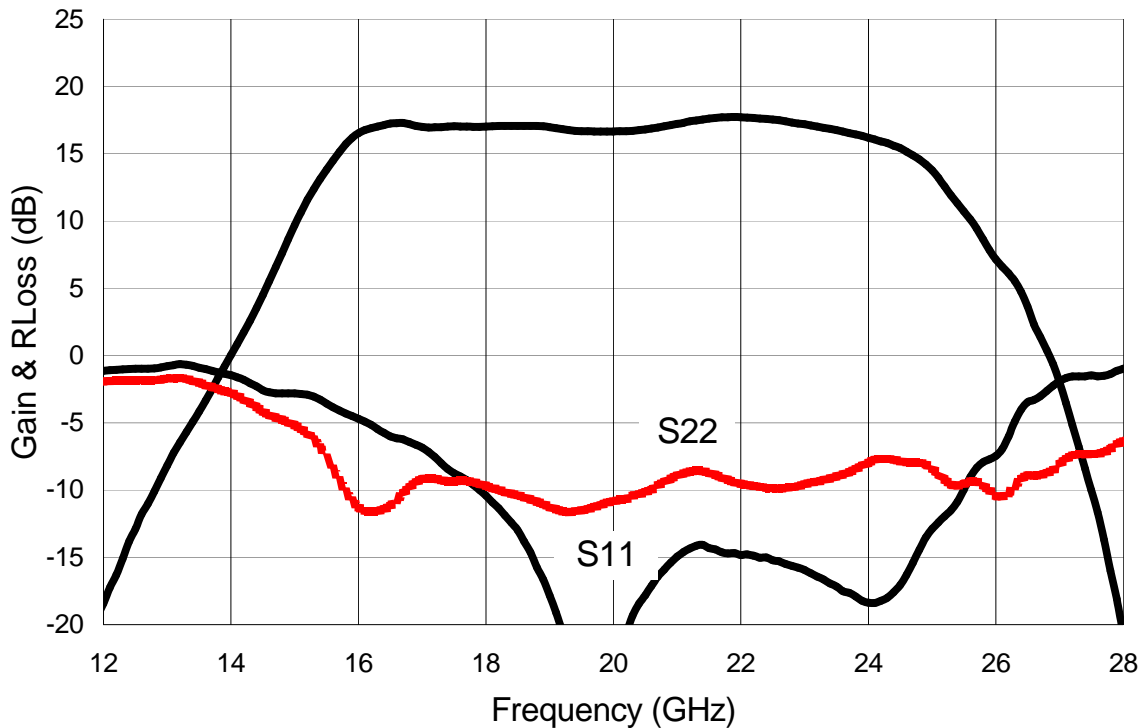
(1) Operation of this device above any one of these parameters may cause permanent damage.

(2) Duration < 1s.

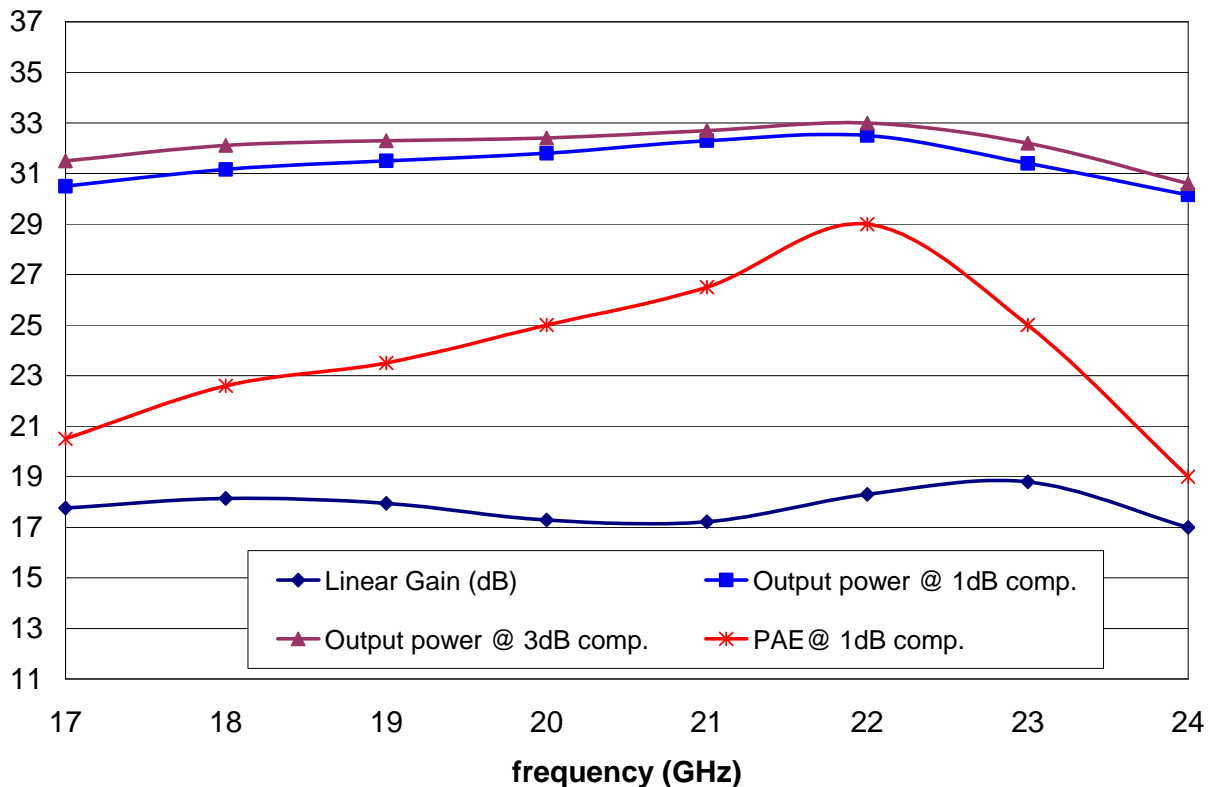
Typical on Jig Measurements

(including 1dB loss for the gain)

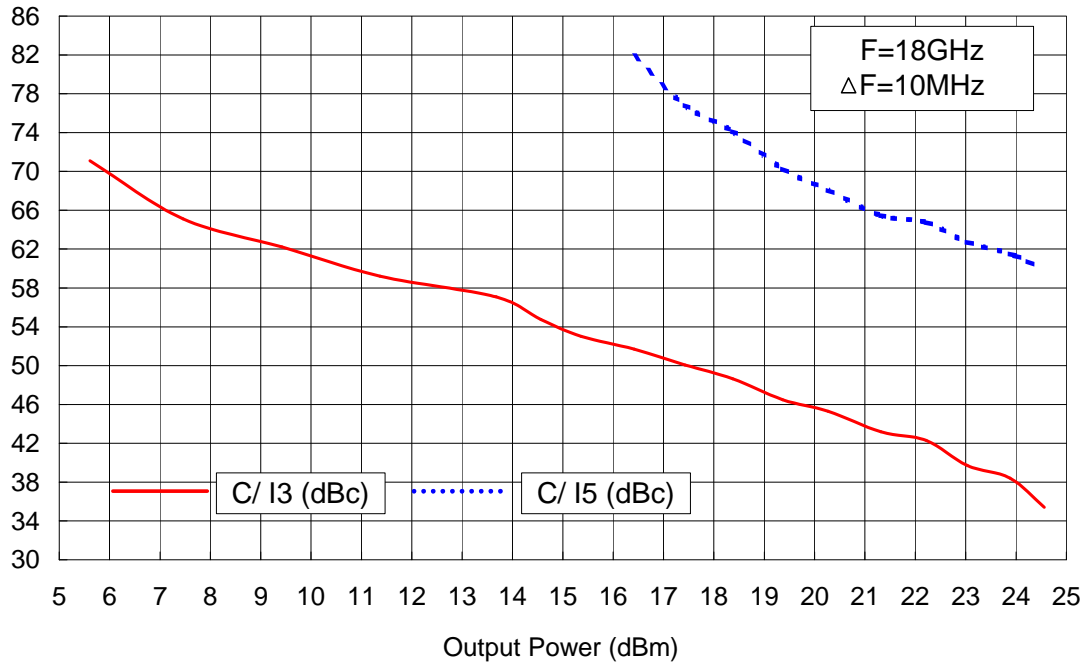
Bias conditions: $V_d=6V$, V_g tuned for $I_d = 800mA$



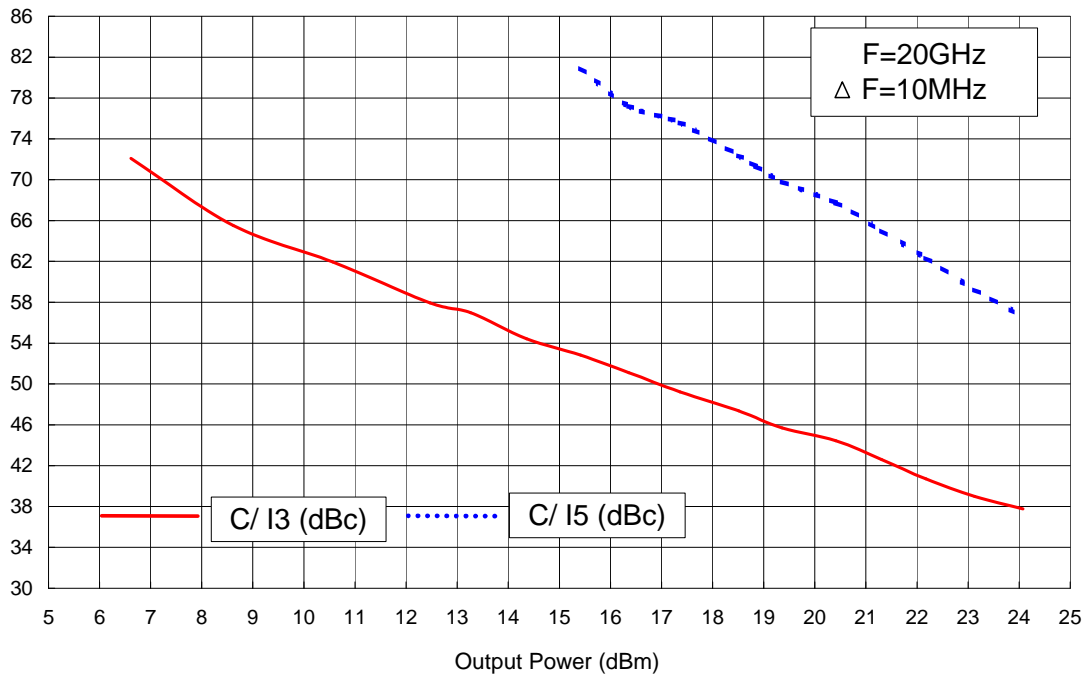
Linear Gain & Return Losses versus frequency



Linear Gain, Output power @ 1dB & 3dB compression, PAE @ 1dB comp.

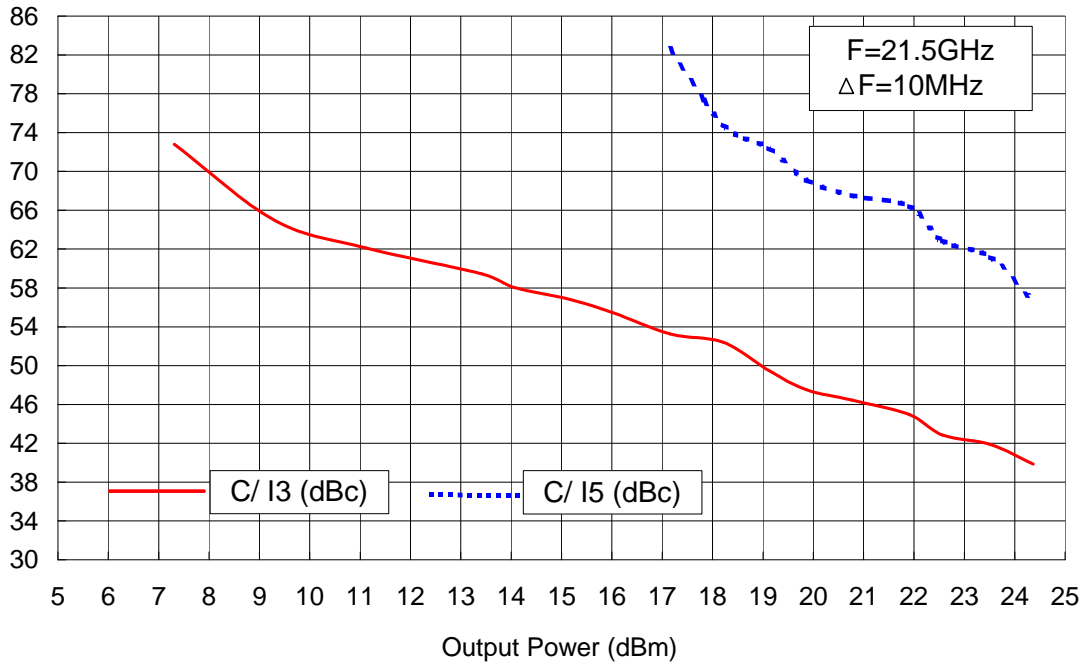


C/I3 & C/I5 versus DCL* output power @ 18GHz

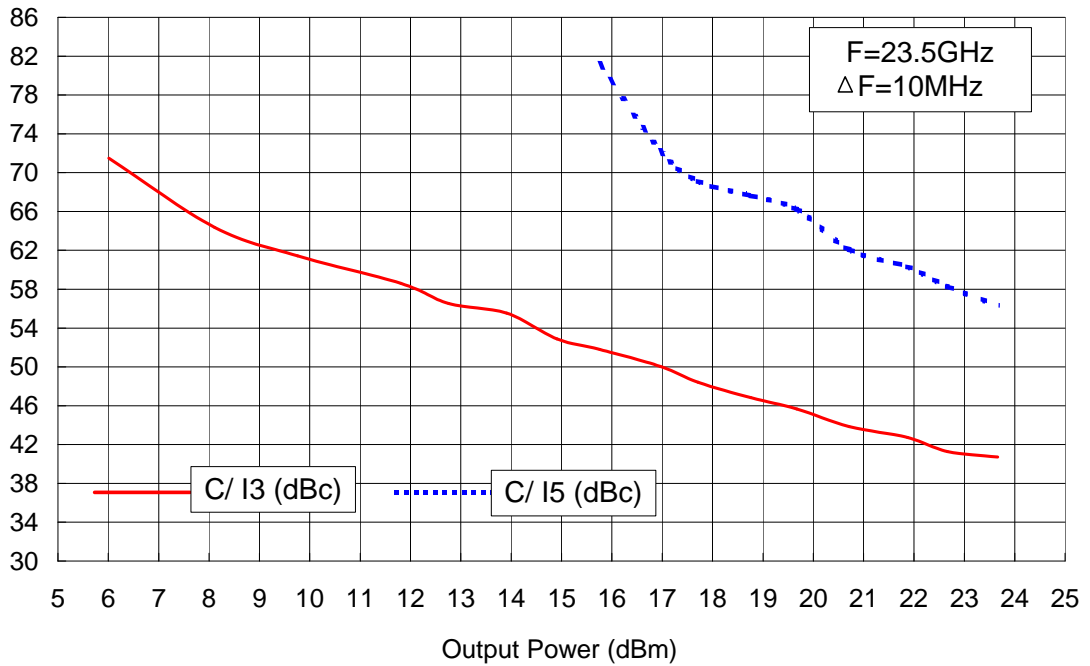


C/I3 & IP3 versus DCLoutput power @ 20GHz

*DCL: Double Carrier Level



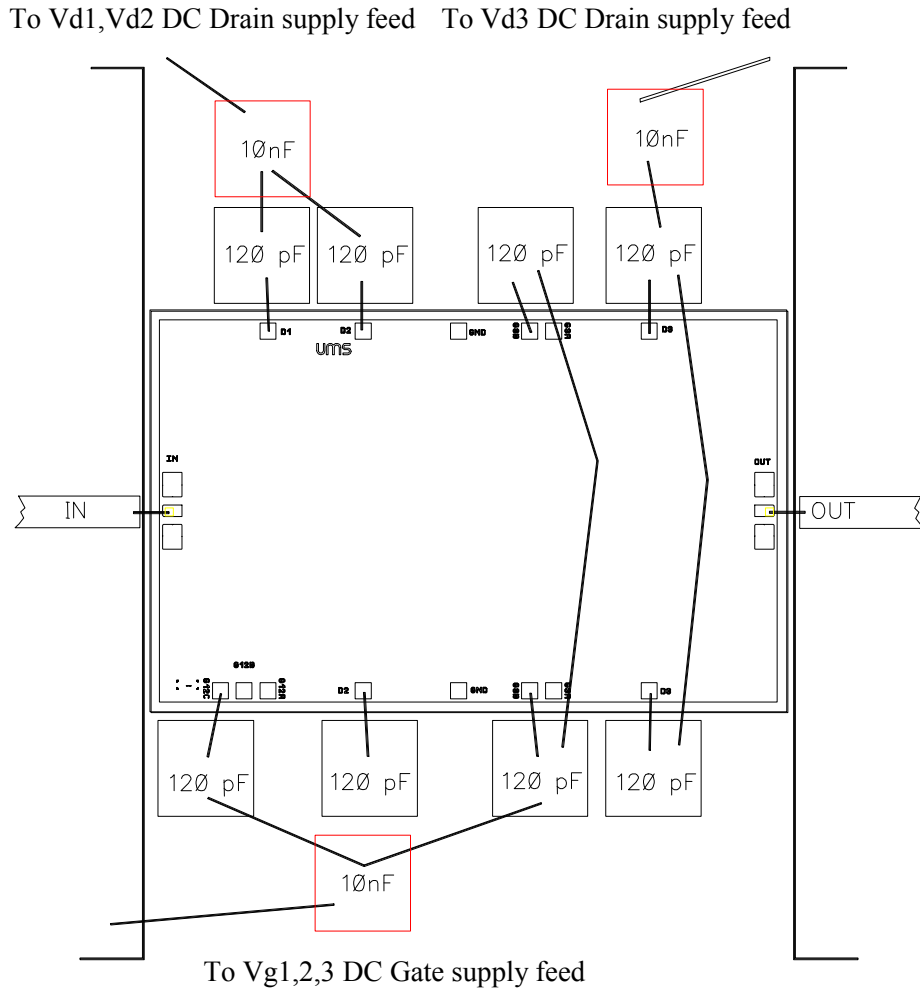
C/I3 & IP3 versus DCL* output power @ 21.5GHz



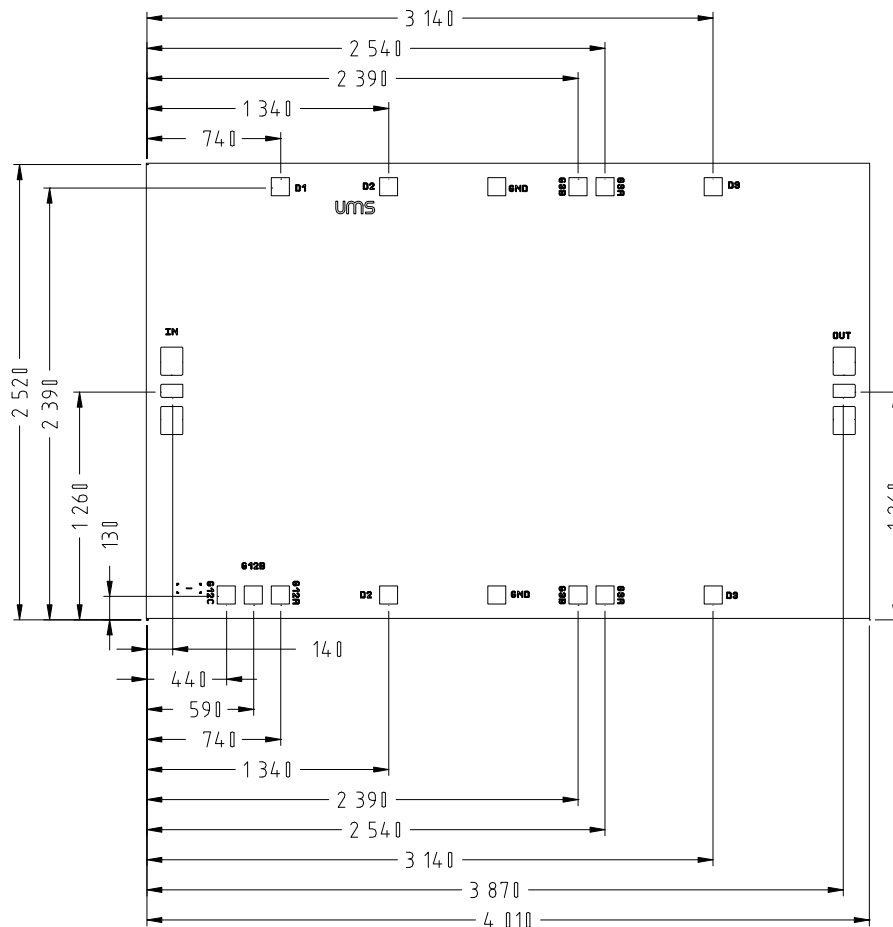
C/I3 & IP3 versus DCL output power @ 23.5GHz

*DCL: Double Carrier Level

Chip Assembly and Mechanical Data



Note : Supply feed should be capacitively bypassed. 25µm diameter gold wire is to be preferred.



UNITS : μm
 Tol : $\pm 35\mu\text{m}$

Bonding pad positions.
 (Chip thickness: $50\mu\text{m}$.)

Application note

Due to $50\mu\text{m}$ thickness, specific care is requested for the handling and assembly.

Bias operation sequence:

- ON: Supply Gate voltage
- Supply Drain voltage
- OFF: Cut off Drain voltage
- Cut off Gate voltage

Ordering Information

Chip form: CHA5293a99F/00

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